



DRV88703.6-A Brushed DC Motor Driver (PWM Control)

1 Features

- H-Bridge Motor Driver
 - Drives One DC Motor, One Winding of a Stepper Motor, or Other Loads
- Wide 6.5-V to 45-V Operating Voltage
- 565-mΩ Typical $R_{DS(on)}$ (HS + LS)
- 3.6-A Peak Current Drive
- PWM Control Interface
- Integrated Current Regulation
- Low-Power Sleep Mode
- Small Package and Footprint
 - 8-Pin HSOP With PowerPAD™
 - 4.9 × 6.0 mm
- **Integrated Protection Features**
 - VM Undervoltage Lockout (UVLO)
 - Overcurrent Protection (OCP)
 - Thermal Shutdown (TSD)
 - Automatic Fault Recovery

2 Applications

- Printers
- Appliances
- Industrial Equipment
- Other Mechatronic Applications

3 Description

The DRV8870 device is a brushed-DC motor driver for printers, appliances, industrial equipment, and other small machines. Two logic inputs control the H-bridge driver, which consists of four N-channel MOSFETs that can control motors bidirectionally with up to 3.6-A peak current. The inputs can be pulse-width modulated (PWM) to control motor speed, using a choice of current-decay modes. Setting both inputs low enters a low-power sleep mode.

The DRV8870 device features integrated current regulation, based on the analog input VREF and the voltage on the ISEN pin, which is proportional to motor current through an external sense resistor. The ability to limit current to a known level can significantly reduce the system power requirements and bulk capacitance needed to maintain stable voltage, especially for motor startup and stall conditions.

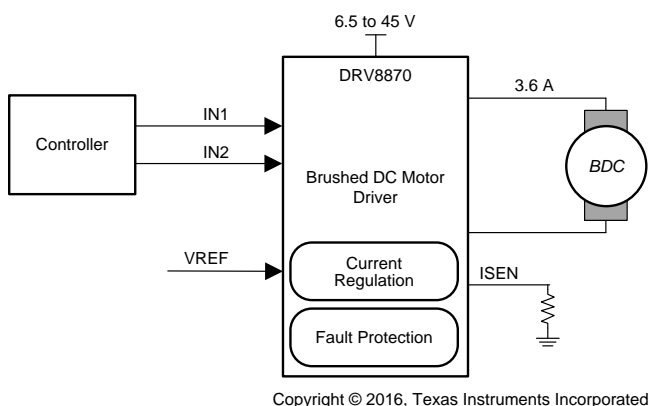
The device is fully protected from faults and short circuits, including undervoltage (UVLO), overcurrent (OCP), and overtemperature (TSD). When the fault condition is removed, the device automatically resumes normal operation.

Device Information ⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|----------|-------------------|
| DRV8870 | HSOP (8) | 4.90 mm × 6.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



H-Bridge States

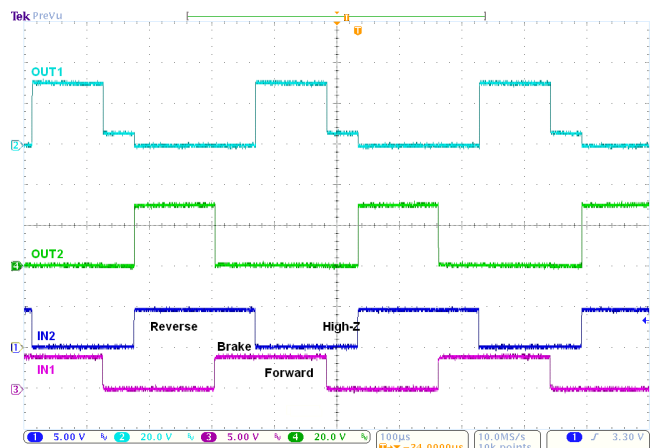


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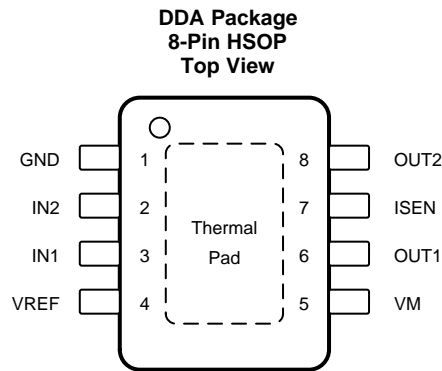
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (January 2016) to Revision B | Page |
|--|-------------|
| • Deleted the power supply voltage ramp rate (VM) parameter from the <i>Absolute Maximum Ratings</i> table | 3 |
| • Added the output current parameter to the <i>Absolute Maximum Ratings</i> table | 3 |
| • Added the <i>Receiving Notification of Documentation Updates</i> section | 17 |

| Changes from Original (August 2015) to Revision A | Page |
|---|-------------|
| • Updated the f_{PWM} max value and added a note | 4 |
| • Removed the redundant T_A condition and added $f_{PWM} = 24$ kHz | 5 |
| • Added more information to clarify how the max RMS current varies for different applications | 12 |

5 Pin Configuration and Functions



Pin Functions

| PIN | | TYPE | DESCRIPTION |
|------|-----|------|---|
| NAME | NO. | | |
| GND | 1 | PWR | Logic ground. Connect to board ground |
| IN1 | 3 | I | Logic inputs. Controls the H-bridge output. Has internal pulldowns. See Table 1 . |
| IN2 | 2 | I | Logic inputs. Controls the H-bridge output. Has internal pulldowns. See Table 1 . |
| ISEN | 7 | PWR | High-current ground path. If using current regulation, connect ISEN to a resistor (low-value, high-power-rating) to ground. If not using current regulation, connect ISEN directly to ground. |
| OUT1 | 6 | O | H-bridge output. Connect directly to the motor or other inductive load. |
| OUT2 | 8 | O | H-bridge output. Connect directly to the motor or other inductive load. |
| VM | 5 | PWR | 6.5-V to 45-V power supply. Connect a 0.1-μF bypass capacitor to ground, as well as sufficient bulk capacitance, rated for the VM voltage. |
| VREF | 4 | I | Analog input. Apply a voltage between 0.3 to 5 V. For information on current regulation, see the Current Regulation section. |
| PAD | | — | Thermal pad. Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes. |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | MIN | MAX | UNIT |
|---|------|----------|------|
| Power supply voltage (VM) | −0.3 | 50 | V |
| Logic input voltage (IN1, IN2) | −0.3 | 7 | V |
| Reference input pin voltage (VREF) | −0.3 | 6 | V |
| Continuous phase node pin voltage (OUT1, OUT2) | −0.7 | VM + 0.7 | V |
| Current sense input pin voltage (ISEN) ⁽²⁾ | −0.5 | 1 | V |
| Output current (100% duty cycle) | 0 | 3.5 | A |
| Operating junction temperature, T _J | −40 | 150 | °C |
| Storage temperature, T _{stg} | −65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Transients of ±1 V for less than 25 ns are acceptable

6.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | |
| | | ±6000 | |
| | | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-------------------|--|--------------------|-----|--------------------|------|
| VM | Power supply voltage | 6.5 | | 45 | V |
| VREF | VREF input voltage | 0.3 ⁽¹⁾ | | 5 | V |
| V _I | Logic input voltage (IN1, IN2) | 0 | | 5.5 | V |
| f _{PWM} | Logic input PWM frequency (IN1, IN2) | 0 | | 200 ⁽²⁾ | kHz |
| I _{peak} | Peak output current ⁽³⁾ | 0 | | 3.6 | A |
| T _A | Operating ambient temperature ⁽³⁾ | –40 | | 125 | °C |

(1) Operational at VREF = 0 to 0.3 V, but accuracy is degraded

(2) The voltages applied to the inputs should have at least 800 ns of pulse width to ensure detection. Typical devices require at least 400 ns. If the PWM frequency is 200 kHz, the usable duty cycle range is 16% to 84%.

(3) Power dissipation and thermal limits must be observed

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | DRV8870 | UNIT |
|-------------------------------|--|------------|------|
| | | DDA (HSOP) | |
| | | 8 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 41.1 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 53.1 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 23.1 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 8.2 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 23 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 2.7 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

$T_A = 25^\circ\text{C}$, over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------------------------|---|-----|-----|------|------------------|
| POWER SUPPLY (VM) | | | | | | |
| VM | VM operating voltage | | 6.5 | | 45 | V |
| I_{VM} | VM operating supply current | VM = 12 V | | 3 | 10 | mA |
| $I_{VMSLEEP}$ | VM sleep current | VM = 12 V | | | 10 | μA |
| $t_{ON}^{(1)}$ | Turn-on time | VM > V_{UVLO} with IN1 or IN2 high | | 40 | 50 | μs |
| LOGIC-LEVEL INPUTS (IN1, IN2) | | | | | | |
| V_{IL} | Input logic low voltage | | | | 0.5 | V |
| V_{IH} | Input logic high voltage | | 1.5 | | | V |
| V_{HYS} | Input logic hysteresis | | | 0.5 | | V |
| I_{IL} | Input logic low current | $V_{IN} = 0\text{ V}$ | –1 | | 1 | μA |
| I_{IH} | Input logic high current | $V_{IN} = 3.3\text{ V}$ | | 33 | 100 | μA |
| R_{PD} | Pulldown resistance | to GND | | 100 | | k Ω |
| t_{PD} | Propagation delay | INx to OUTx change (see Figure 6) | | 0.7 | 1 | μs |
| t_{sleep} | Time to sleep | Inputs low to sleep | | 1 | 1.5 | ms |
| MOTOR DRIVER OUTPUTS (OUT1, OUT2) | | | | | | |
| $R_{DS(ON)}$ | High-side FET on resistance | VM = 24 V, $I = 1\text{ A}$, $f_{PWM} = 25\text{ kHz}$ | | 307 | 360 | m Ω |
| $R_{DS(ON)}$ | Low-side FET on resistance | VM = 24 V, $I = 1\text{ A}$, $f_{PWM} = 25\text{ kHz}$ | | 258 | 320 | m Ω |
| t_{DEAD} | Output dead time | | | 220 | | ns |
| V_d | Body diode forward voltage | $I_{OUT} = 1\text{ A}$ | | 0.8 | 1 | V |
| CURRENT REGULATION | | | | | | |
| A_V | ISEN gain | $V_{REF} = 2.5\text{ V}$ | 9.4 | 10 | 10.4 | V/V |
| t_{OFF} | PWM off-time | | | 25 | | μs |
| t_{BLANK} | PWM blanking time | | | 2 | | μs |
| PROTECTION CIRCUITS | | | | | | |
| V_{UVLO} | VM undervoltage lockout | VM falls until UVLO triggers | | 6.1 | 6.4 | V |
| | | VM rises until operation recovers | | 6.3 | 6.5 | |
| $V_{UV,HYS}$ | VM undervoltage hysteresis | Rising to falling threshold | 100 | 180 | | mV |
| I_{OCP} | Overcurrent protection trip level | | 3.7 | 4.5 | 6.4 | A |
| t_{OCP} | Overcurrent deglitch time | | | 1.5 | | μs |
| t_{RETRY} | Overcurrent retry time | | | 3 | | ms |
| T_{SD} | Thermal shutdown temperature | | 150 | 175 | | $^\circ\text{C}$ |
| T_{HYS} | Thermal shutdown hysteresis | | | 40 | | $^\circ\text{C}$ |

(1) t_{ON} applies when the device initially powers up, and when it exits sleep mode.

6.6 Typical Characteristics

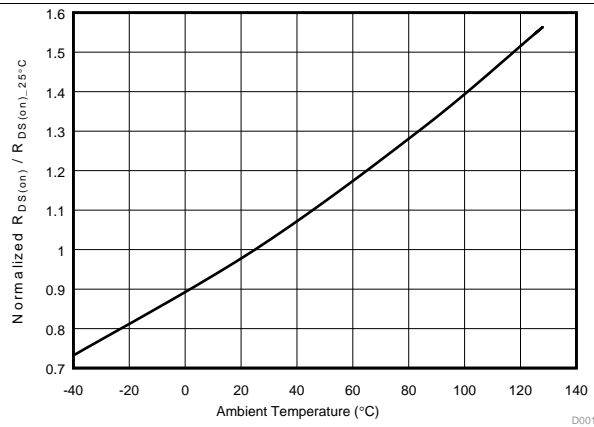


Figure 1. $R_{DS(on)}$ vs Temperature

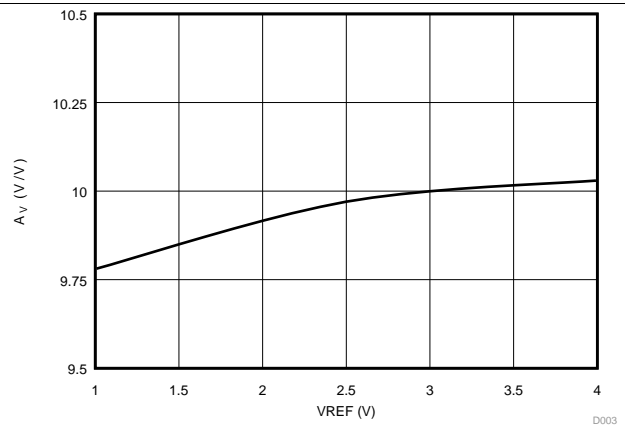


Figure 2. A_V vs VREF

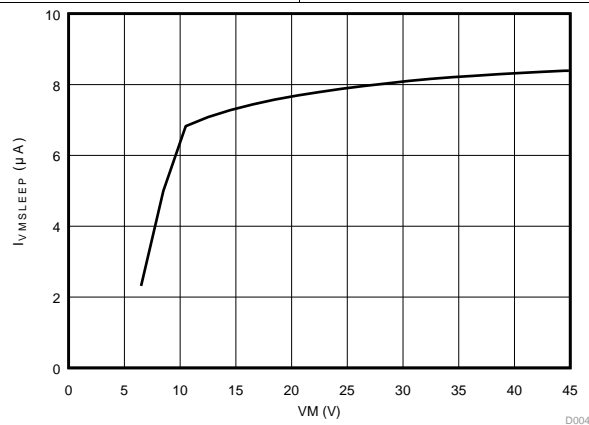


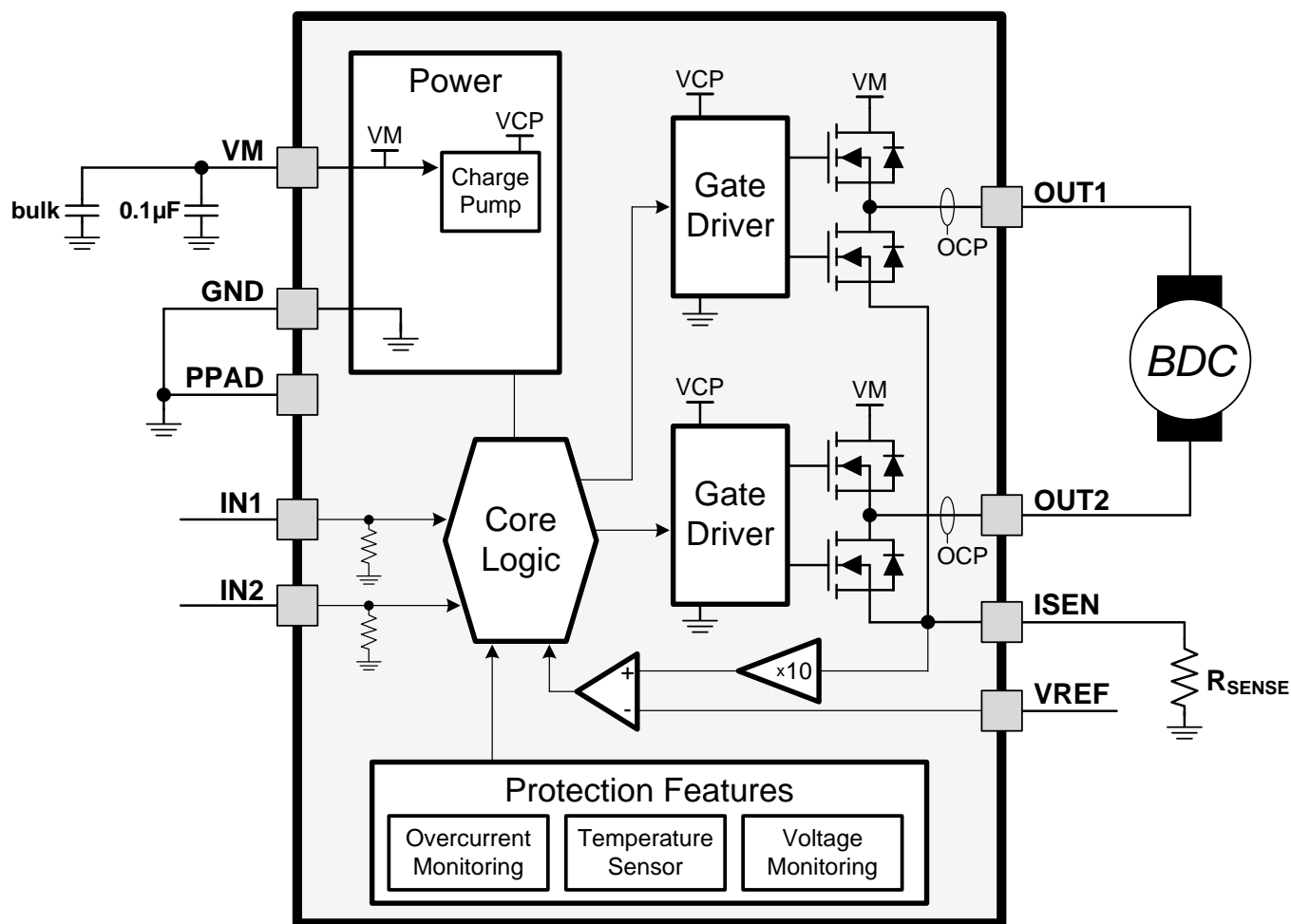
Figure 3. $I_{VMSLEEP}$ vs VM at 25°C

7 Detailed Description

7.1 Overview

The DRV8870 device is an optimized 8-pin device for driving brushed DC motors with 6.5 to 45 V and up to 3.6-A peak current. The integrated current regulation restricts motor current to a predefined maximum. Two logic inputs control the H-bridge driver, which consists of four N-channel MOSFETs that have a typical $R_{ds(on)}$ of 565 m Ω (including one high-side and one low-side FET). A single-power input, VM, serves as both device power and the motor winding bias voltage. The integrated charge pump of the device boosts VM internally and fully enhances the high-side FETs. Motor speed can be controlled with pulse-width modulation, at frequencies between 0 to 100 kHz. The device has an integrated sleep mode that is entered by bringing both inputs low. An assortment of protection features prevent the device from being damaged if a system fault occurs.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Bridge Control

The DRV8870 output consists of four N-channel MOSFETs that are designed to drive high current. These outputs are controlled by the two logic inputs IN1 and IN2 as listed in [Table 1](#).

Table 1. H-Bridge Control

| IN1 | IN2 | OUT1 | OUT2 | DESCRIPTION |
|-----|-----|--------|--------|---|
| 0 | 0 | High-Z | High-Z | Coast; H-bridge disabled to High-Z (sleep entered after 1 ms) |
| 0 | 1 | L | H | Reverse (Current OUT2 → OUT1) |
| 1 | 0 | H | L | Forward (Current OUT1 → OUT2) |
| 1 | 1 | L | L | Brake; low-side slow decay |

The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM, switching between driving and braking typically works best. For example, to drive a motor forward with 50% of the maximum RPM, IN1 = 1 and IN2 = 0 during the driving period, and IN1 = 1 and IN2 = 1 during the other period. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for *fast current decay* is also available. The input pins can be powered before VM is applied.

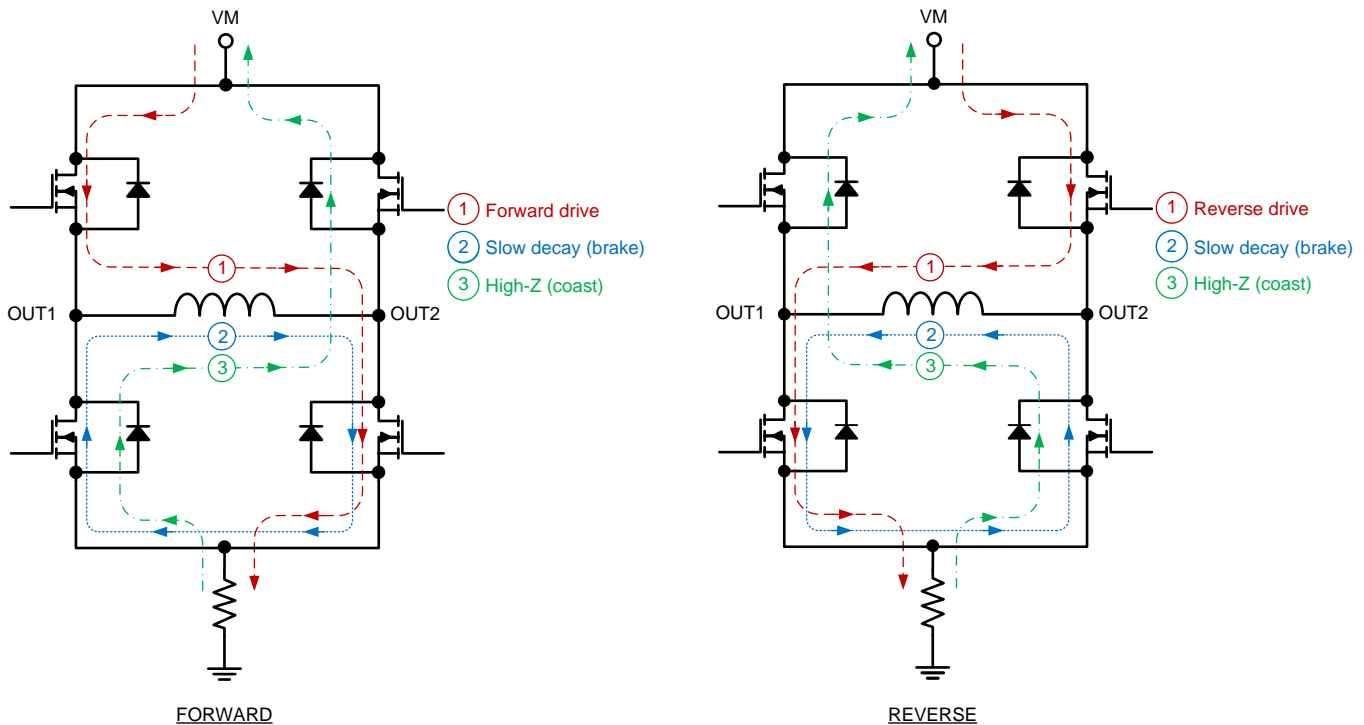


Figure 4. H-Bridge Current Paths

7.3.2 Sleep Mode

When the IN1 and IN2 pins are both low for time t_{SLEEP} (typically 1 ms), the DRV8870 device enters a low-power sleep mode, where the outputs remain High-Z and the device uses $I_{VMSLEEP}$ (μA) of current. If the device is powered up while both inputs are low, it immediately enters sleep mode. After the IN1 or IN2 pins are high for at least 5 μs , the device is operational 50 μs (t_{ON}) later.

7.3.3 Current Regulation

The DRV8870 device limits the output current based on the analog input, VREF, and the resistance of an external sense resistor on the ISEN pin according to [Equation 1](#):

$$I_{TRIP} (A) = \frac{VREF (V)}{A_V \times R_{ISEN} (\Omega)} = \frac{VREF (V)}{10 \times R_{ISEN} (\Omega)} \quad (1)$$

For example, if $VREF = 3.3 V$ and a $R_{ISEN} = 0.15 \Omega$, the DRV8870 device limits motor current to 2.2 A no matter how much load torque is applied. For guidelines on selecting a sense resistor, see the [Sense Resistor](#) section.

When I_{TRIP} is reached, the device enforces slow current decay by enabling both low-side FETs, and it does this for a time of t_{OFF} (typically 25 μs).

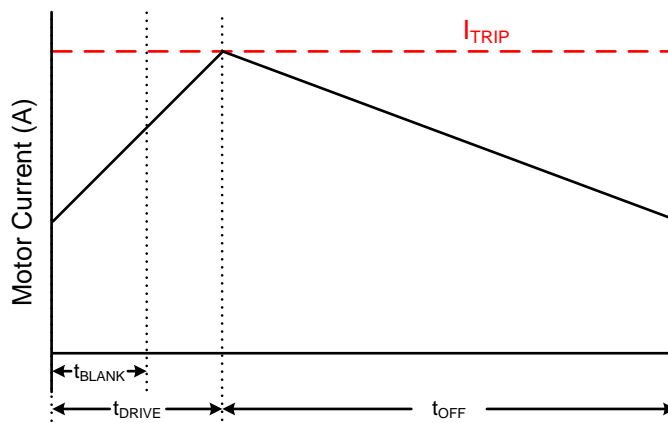


Figure 5. Current-Regulation Time Periods

After t_{OFF} elapses, the output is re-enabled according to the two inputs, INx . The drive time (t_{DRIVE}) until reaching another I_{TRIP} event heavily depends on the VM voltage, the back-EMF of the motor, and the inductance of the motor.

7.3.4 Dead Time

When an output changes from driving high to driving low, or driving low to driving high, dead time is automatically inserted to prevent shoot-through. The t_{DEAD} time is the time in the middle when the output is High-Z. If the output pin is measured during t_{DEAD} , the voltage depends on the direction of current. If the current is leaving the pin, the voltage is a diode drop below ground. If the current is entering the pin, the voltage is a diode drop above VM. This diode is the body diode of the high-side or low-side FET.

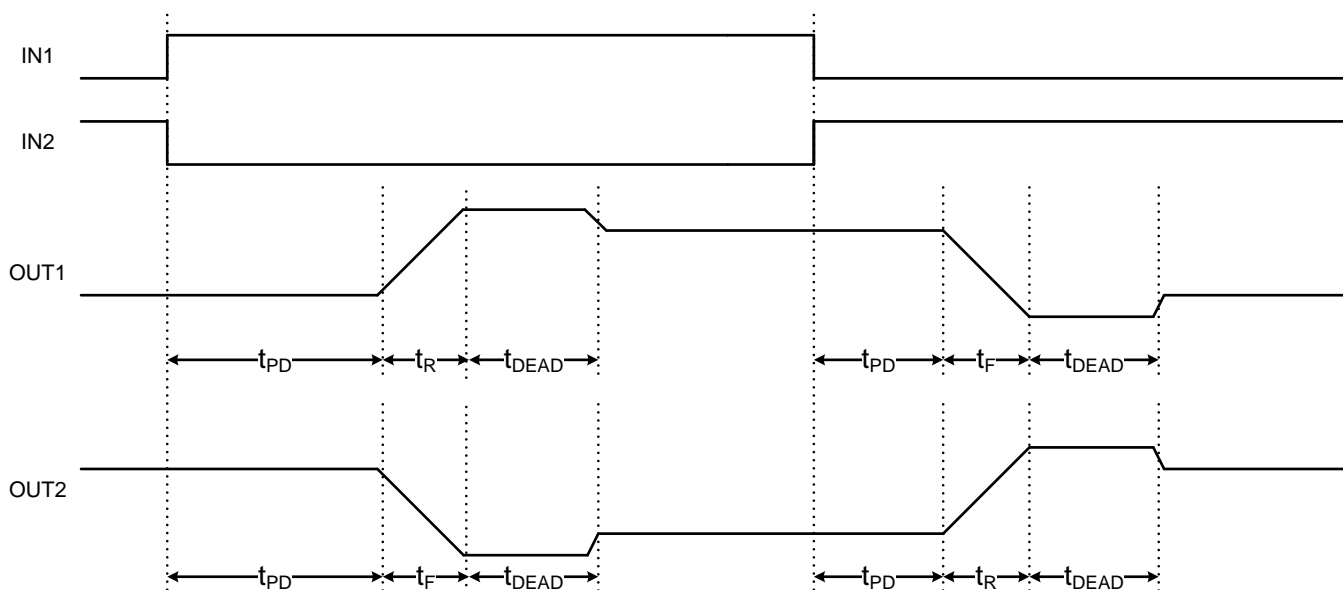


Figure 6. Propagation Delay Time

7.3.5 Protection Circuits

The DRV8870 device is fully protected against VM undervoltage, overcurrent, and overtemperature events.

7.3.5.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage-lockout threshold voltage, all FETs in the H-bridge will be disabled. Operation resumes when VM rises above the UVLO threshold.

7.3.5.2 Overcurrent Protection (OCP)

If the output current exceeds the OCP threshold, I_{OCP} , for longer than t_{OCP} , all FETs in the H-bridge are disabled for a duration of t_{RETRY} . After that, the H-bridge is re-enabled according to the state of the INx pins. If the overcurrent fault is still present, the cycle repeats; otherwise normal device operation resumes.

7.3.5.3 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature has fallen to a safe level, operation automatically resumes.

Table 2. Protection Functionality

| FAULT | CONDITION | H-BRIDGE BECOMES | RECOVERY |
|--------------------------------|----------------------|------------------|--------------------------|
| VM undervoltage lockout (UVLO) | $VM < V_{UVLO}$ | Disabled | $VM > V_{UVLO}$ |
| Overcurrent (OCP) | $I_{OUT} > I_{OCP}$ | Disabled | t_{RETRY} |
| Thermal Shutdown (TSD) | $T_J > 150^{\circ}C$ | Disabled | $T_J < T_{SD} - T_{HYS}$ |

7.4 Device Functional Modes

The DRV8870 device can be used in multiple ways to drive a brushed DC motor.

7.4.1 PWM With Current Regulation

This scheme uses all of the capabilities of the device. The I_{TRIP} current is set above the normal operating current, and high enough to achieve an adequate spin-up time, but low enough to constrain current to a desired level. Motor speed is controlled by the duty cycle of one of the inputs, while the other input is static. Brake or slow decay is typically used during the off-time.

7.4.2 PWM Without Current Regulation

If current regulation is not required, the ISEN pin should be directly connected to the PCB ground plane. The VREF voltage must still be 0.3 to 5 V, and larger voltages provide greater noise margin. This mode provides the highest-possible peak current which is up to 3.6 A for a few hundred milliseconds (depending on PCB characteristics and the ambient temperature). If current exceeds 3.6 A, the device might reach overcurrent protection (OCP) or overtemperature shutdown (TSD). If that happens, the device disables and protects itself for about 3 ms (t_{RETRY}) and then resumes normal operation.

7.4.3 Static Inputs With Current Regulation

The IN1 and IN2 pins can be set high and low for 100% duty cycle drive, and I_{TRIP} can be used to control the current of the motor, speed, and torque capability.

7.4.4 VM Control

In some systems, varying VM as a means of changing motor speed is desirable. See the [Motor Voltage](#) section for more information.

8 Application and Implementation

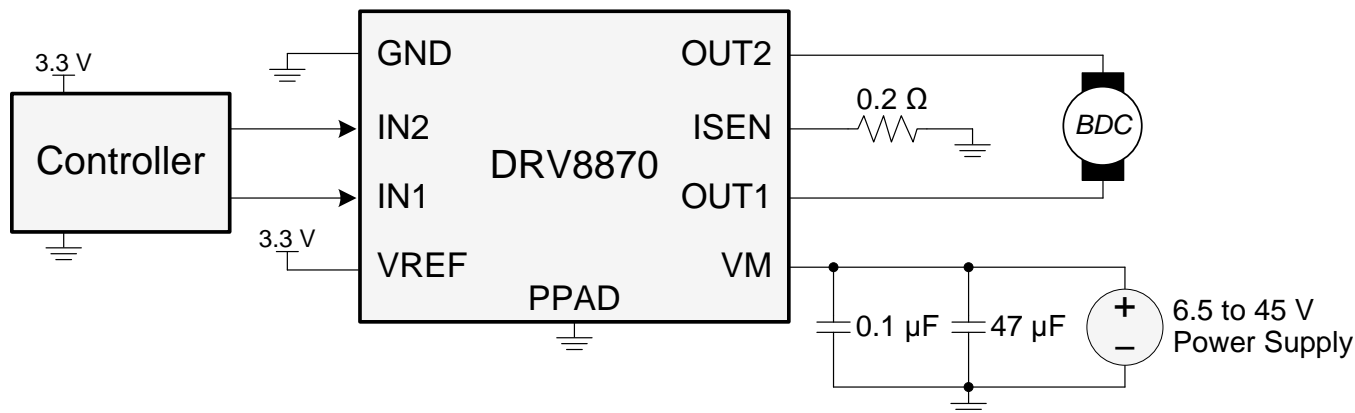
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8870 device is typically used to drive one brushed DC motor.

8.2 Typical Application



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Figure 7. Typical Connections

8.2.1 Design Requirements

Table 3 lists the design parameters.

Table 3. Design Parameters

| DESIGN PARAMETER | REFERENCE | EXAMPLE VALUE |
|--------------------------|-------------|---------------|
| Motor voltage | V_M | 24 V |
| Motor RMS current | I_{RMS} | 0.8 A |
| Motor startup current | I_{START} | 2 A |
| Motor current trip point | I_{TRIP} | 2.2 A |
| VREF voltage | VREF | 3.3 V |
| Sense resistance | R_{ISEN} | 0.15 Ω |
| PWM frequency | f_{PWM} | 5 kHz |

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The motor voltage to use depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.2.2 Drive Current

The current path is through the high-side sourcing DMOS power driver, motor winding, and low-side sinking DMOS power driver. Power dissipation losses in one source and sink DMOS power driver are shown in Equation 2.

$$P_D = I^2 (R_{DS(on)Source} + R_{DS(on)Sink}) \quad (2)$$

The DRV8870 device has been measured to be capable of 2-A RMS current at 25°C on standard FR-4 PCBs. The maximum RMS current varies based on the PCB design, ambient temperature, and PWM frequency. Typically, switching the inputs at 200 kHz compared to 20 kHz causes 20% more power loss in heat.

8.2.2.3 Sense Resistor

For optimal performance, the sense resistor must have the following characteristics:

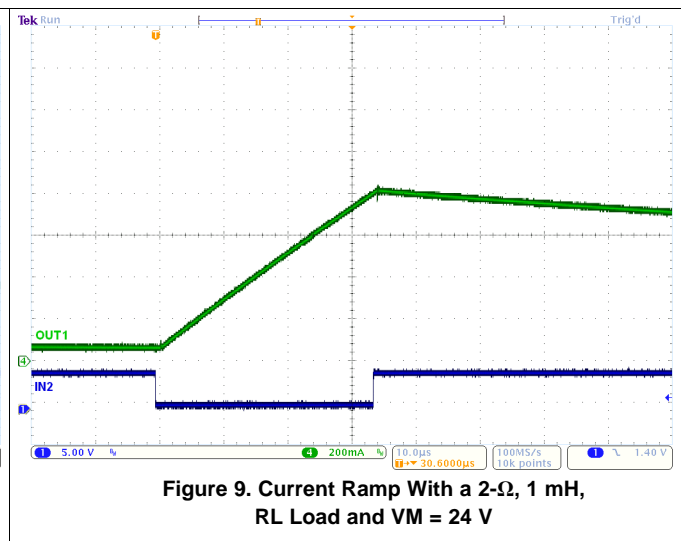
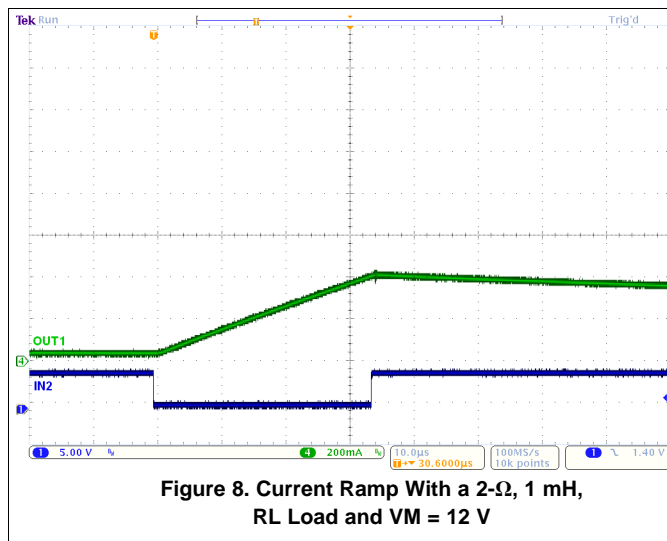
- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

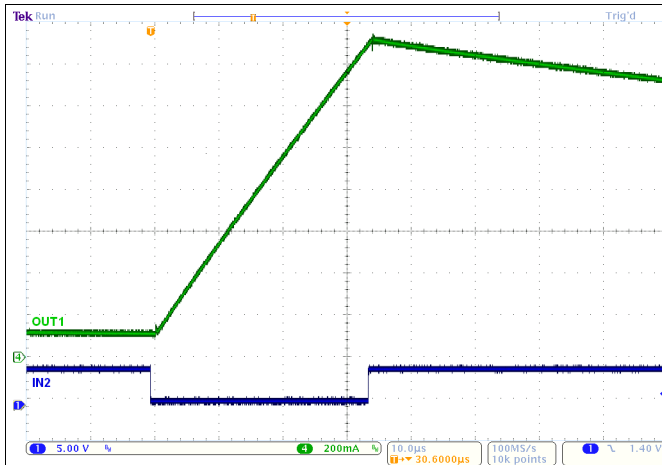
The power dissipated by the sense resistor equals $I_{RMS}^2 \times R$. For example, if peak motor current is 3 A, RMS motor current is 1.5 A, and a 0.2-Ω sense resistor is used, the resistor dissipates $1.5 A^2 \times 0.2 \Omega = 0.45 W$. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, the system designer should add margin. Measuring the actual sense resistor temperature in a final system is always best.

Because power resistors are larger and more expensive than standard resistors, using multiple standard resistors in parallel, between the sense node and ground, is common and distributes the current and heat dissipation.

8.2.3 Application Curves





**Figure 10. Current Ramp With a 2-Ω, 1 mH,
RL Load and VM = 45 V**

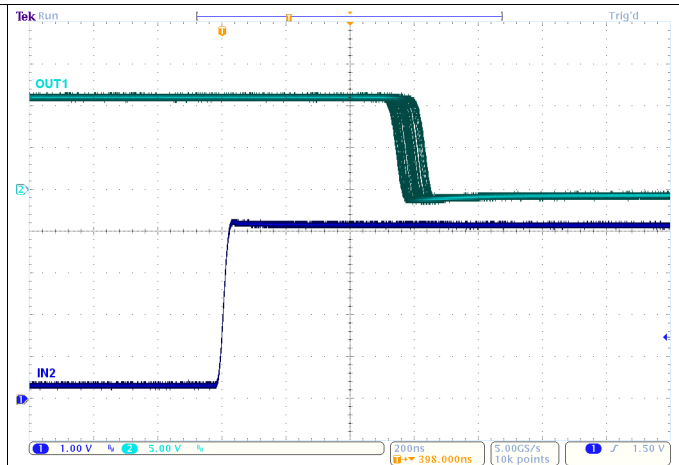
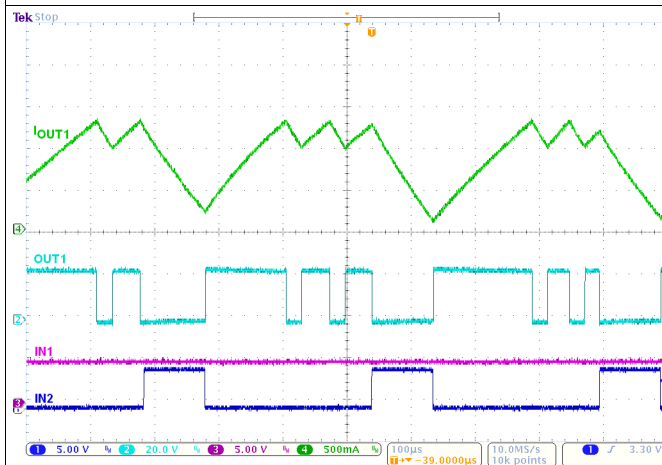
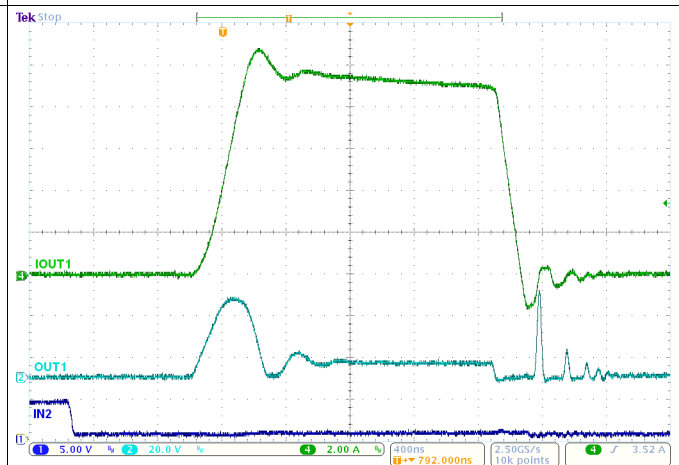


Figure 11. t_{PD}



**Figure 12. Current Regulation With VREF = 2 V and
150 mΩ**



**Figure 13. OCP With 45 V and the Outputs Shorted
Together**

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance of the power supply and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits how the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

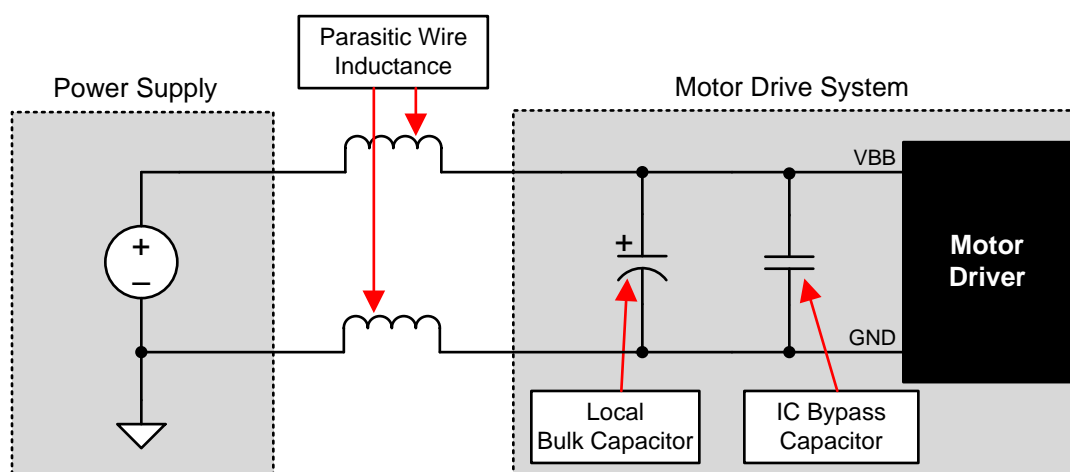


Figure 14. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

10.2 Layout Example

Figure 15 shows the recommended layout and component placement.

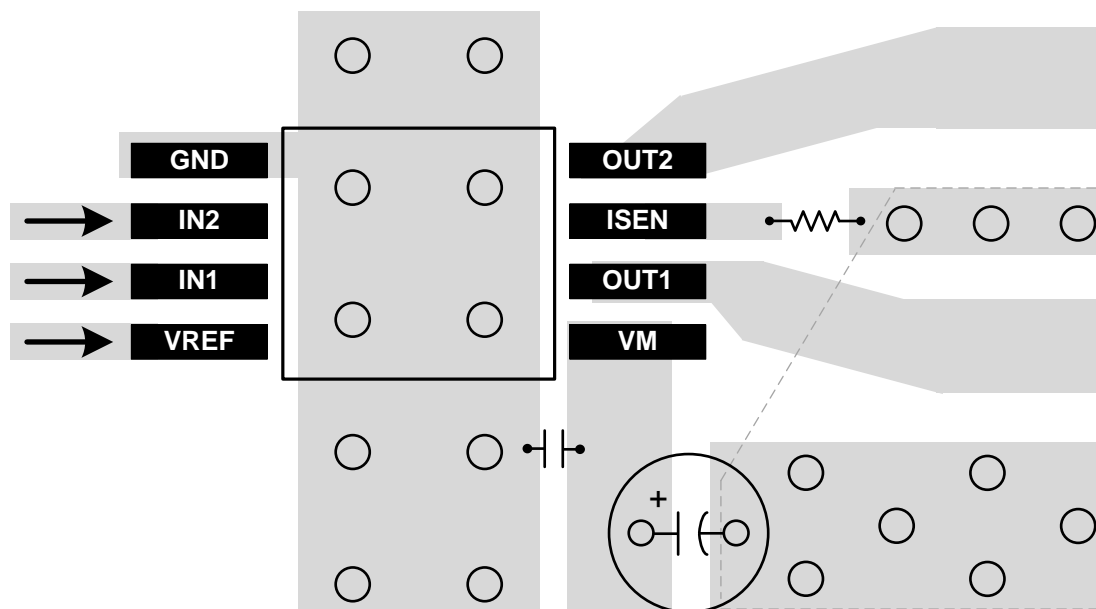


Figure 15. Layout Recommendation

10.3 Thermal Considerations

The DRV8870 device has thermal shutdown (TSD) as described in the [Thermal Shutdown \(TSD\)](#) section. If the die temperature exceeds approximately 175°C, the device is disabled until the temperature drops below the temperature hysteresis level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high of an ambient temperature.

10.4 Power Dissipation

Power dissipation in the DRV8870 device is dominated by the power dissipated in the output FET resistance, $R_{DS(on)}$. Use the equation in the [Drive Current](#) section to calculate the estimated average power dissipation when driving a load.

Note that at startup, the current is much higher than normal running current; this peak current and its duration must be also be considered.

Power Dissipation (continued)

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

NOTE

$R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. This fact must be taken into consideration when sizing the heatsink.

The power dissipation of the DRV8870 device is a function of RMS motor current and the FET resistance ($R_{DS(ON)}$) of each output.

$$\text{Power} \approx I_{RMS}^2 \times (\text{High-side } R_{DS(ON)} + \text{Low-side } R_{DS(ON)}) \quad (3)$$

For this example, the ambient temperature is 58°C, and the junction temperature reaches 80°C. At 58°C, the sum of $R_{DS(ON)}$ is about 0.72 Ω . With an example motor current of 0.8 A, the dissipated power in the form of heat is $0.8 \text{ A}^2 \times 0.72 \Omega = 0.46 \text{ W}$.

The temperature that the DRV8870 reaches will depend on the thermal resistance to the air and PCB. It is important to solder the device PowerPAD to the PCB ground plane, with vias to the top and bottom board layers, in order dissipate heat into the PCB and reduce the device temperature. In the example used here, the DRV8870 device had an effective thermal resistance $R_{\theta JA}$ of 48°C/W, and:

$$T_J = T_A + (P_D \times R_{\theta JA}) = 58^\circ\text{C} + (0.46 \text{ W} \times 48^\circ\text{C/W}) = 80^\circ\text{C} \quad (4)$$

10.4.1 Heatsinking

The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this connection can be accomplished by adding a number of vias to connect the thermal pad to the ground plane.

On PCBs without internal planes, a copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to [PowerPAD™ Thermally Enhanced Package](#) and [PowerPAD Made Easy™](#), available at www.ti.com. In general, the more copper area that can be provided, the more power can be dissipated.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- [Calculating Motor Driver Power Dissipation](#)
- [Current Recirculation and Decay Modes](#)
- [PowerPAD™ Made Easy](#)
- [PowerPAD™ Thermally Enhanced Package](#)
- [Understanding Motor Driver Current Ratings](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| DRV8870DDA | OBSOLETE | SO PowerPAD | DDA | 8 | | TBD | Call TI | Call TI | -40 to 125 | 8870 | |
| DRV8870DDAR | ACTIVE | SO PowerPAD | DDA | 8 | 2500 | RoHS & Green | NIPDAU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 8870 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DRV8870DDAR | SO PowerPAD | DDA | 8 | 2500 | 330.0 | 12.5 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DRV8870DDAR | SO PowerPAD | DDA | 8 | 2500 | 353.0 | 353.0 | 32.0 |



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA0008B

PACKAGE OUTLINE

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4214849/A 08/2016

NOTES:

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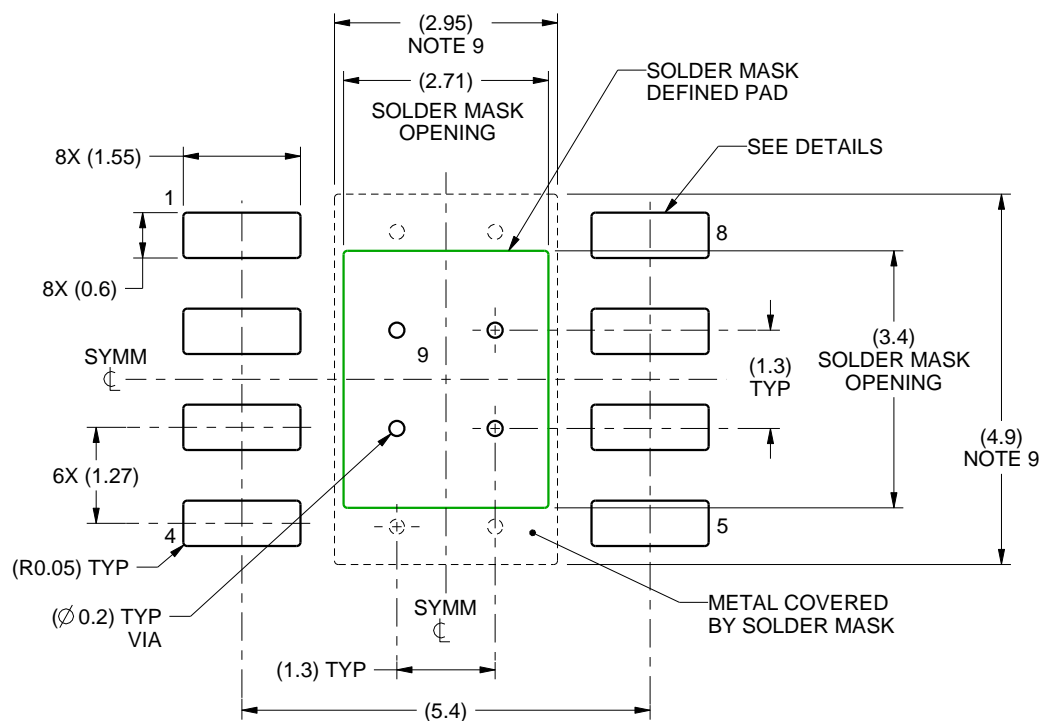
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

EXAMPLE BOARD LAYOUT

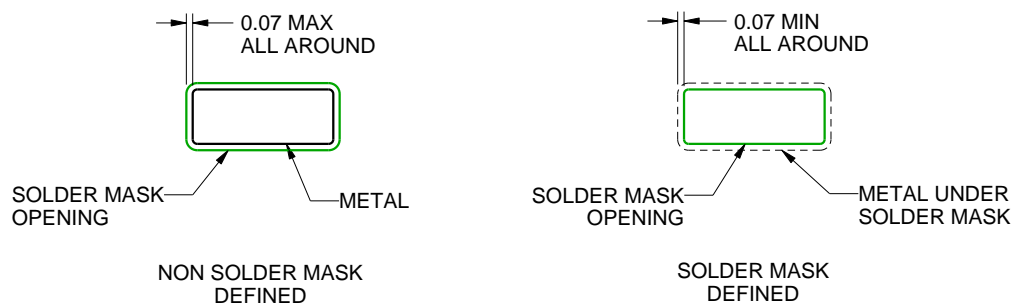
DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

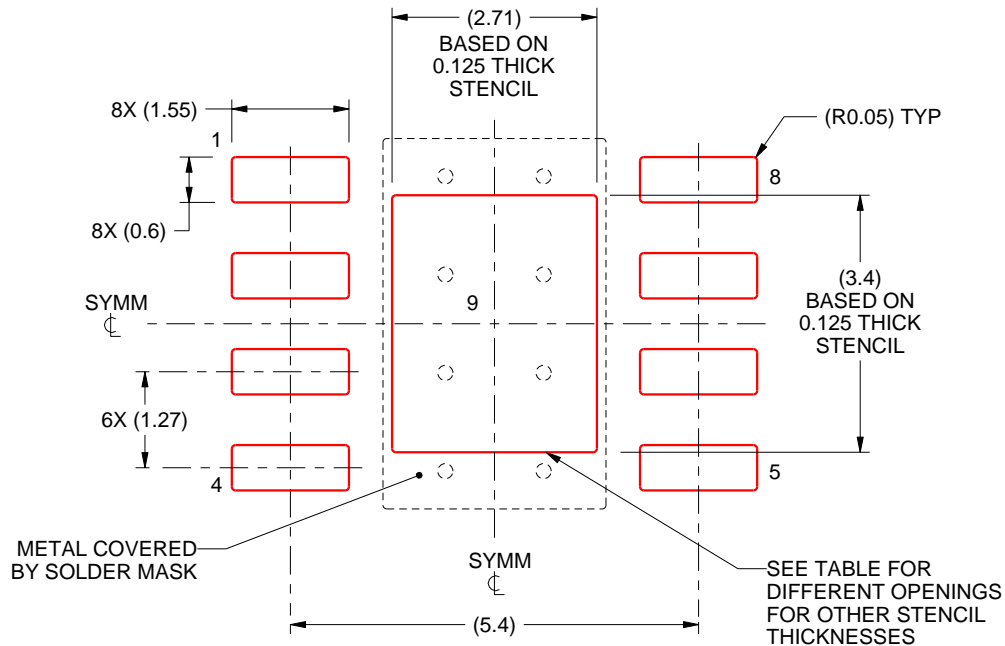
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1 | 3.03 X 3.80 |
| 0.125 | 2.71 X 3.40 (SHOWN) |
| 0.150 | 2.47 X 3.10 |
| 0.175 | 2.29 X 2.87 |

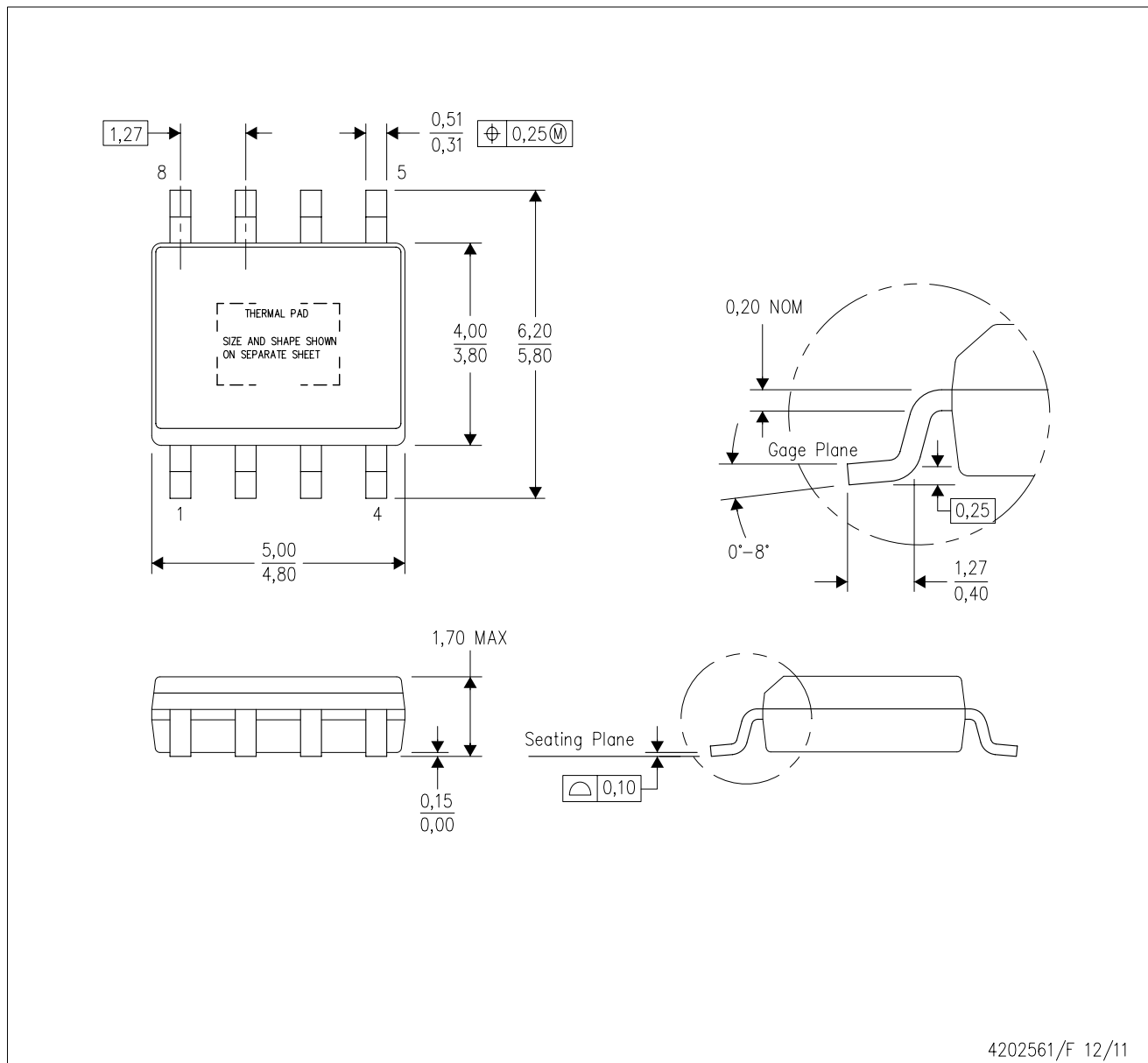
4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - This package complies to JEDEC MS-012 variation BA

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DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



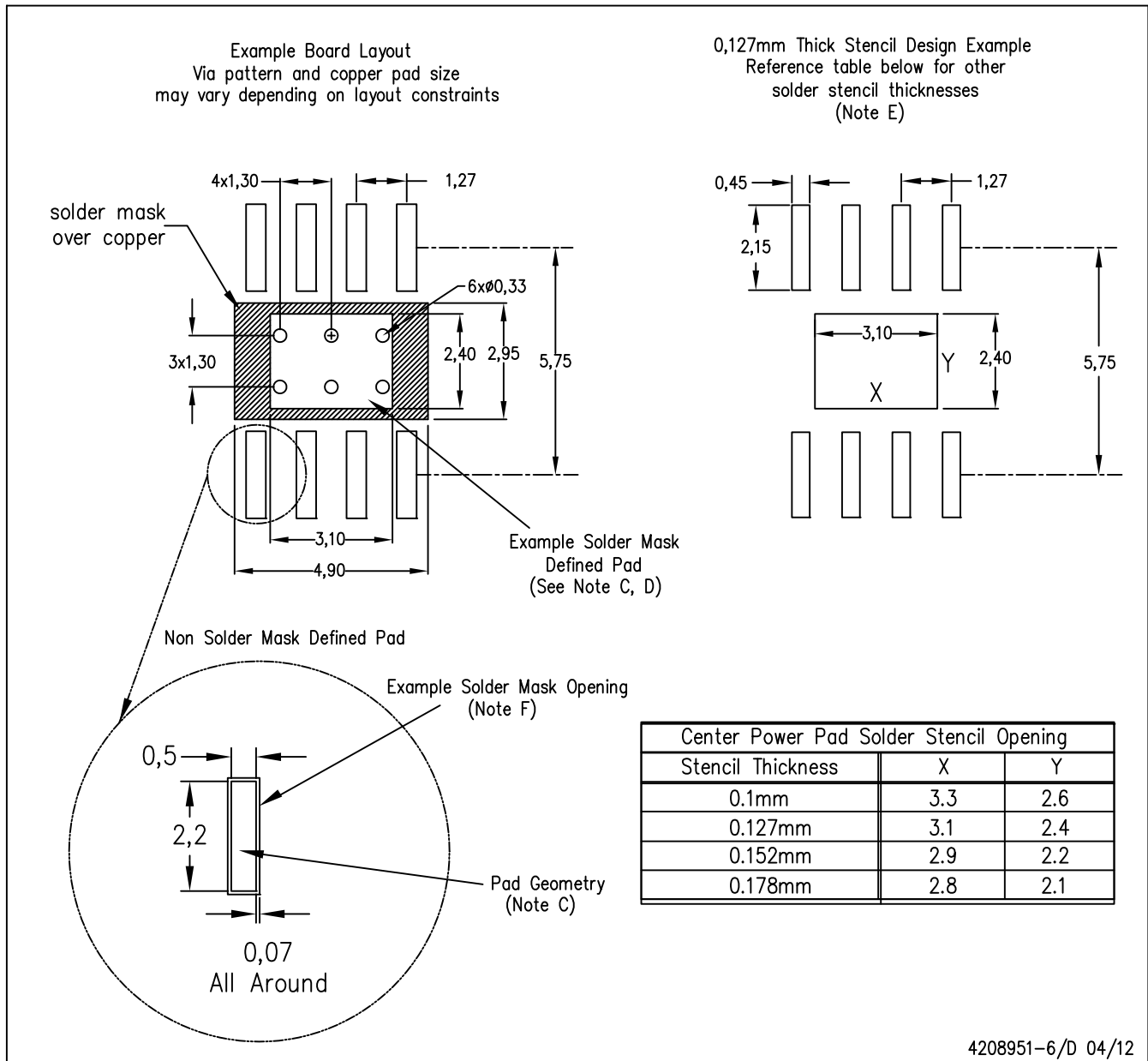
4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

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DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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