Radiation-Tolerant Isolated DC-to-DC Converter

LE50-28 Triple Series

Introduction

The LE50-28 is an isolated DC-to-DC converter capable of delivering up to 50W of output power in a small size design. The LE family provides a radiation-tolerant option with top class TID and SEE performance for space and military applications. With forward converter topology and a patented magnetic feedback, the LE50-28 is optimized for applications where isolated DC voltage conversion is required. The discrete surface mount design facilitates customization with reasonable lead time and modest NRE cost.

To achieve MIL-STD-461 EMI compliance, an external filter is required. Off-the-shelf filters, such as Microchip's SF100-28-28S, are available.

As a non-hybrid space-grade DC-DC power converter module in the market, the LE50-28 series excels in its robustness in applications with $1x10^6$ hours of MTBF.

The LE50-28 is available in a 3.055" x 2.055" x 0.5" package.

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1. Benefits and Features

- Up to 50W Output Power
- 22 VDC to 38 VDC Input Range
- Four Output Configurations Available

Table 1-1. Output Configurations

Main	Aux A/B	Base Part Number
3.3V	12V	LE50-28-3R3-12T
3.3V	15V	LE50-28-3R3-15T
5V	12V	LE50-28-5-12T
5V	15V	LE50-28-5-15T

- Dual Isolated 12V or 15V Auxiliary Outputs
- Up to 82% Efficiency @ Full Load
- <1% Output Ripple
- Forward Topology
- Patented Magnetic Feedback
- Inhibit Pin for Electrical ON/OFF
- Isolated Synchronization Input
- Low Mass 120g
- Flight Proven Technology with >1 x 10^6 Hours of MTBF
- Product is Classified as EAR99
- Customization of Input/Output Voltages Available Upon Request

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2. Radiation Performance

- TID >50 krad (Si) and 30 krad (Si) ELDRS (<10 mrad/s) per MIL-STD-883 Method 1019
- SEE (SEGR, SEB, SET, SEL) immunity >37 MeV·cm^2/mg

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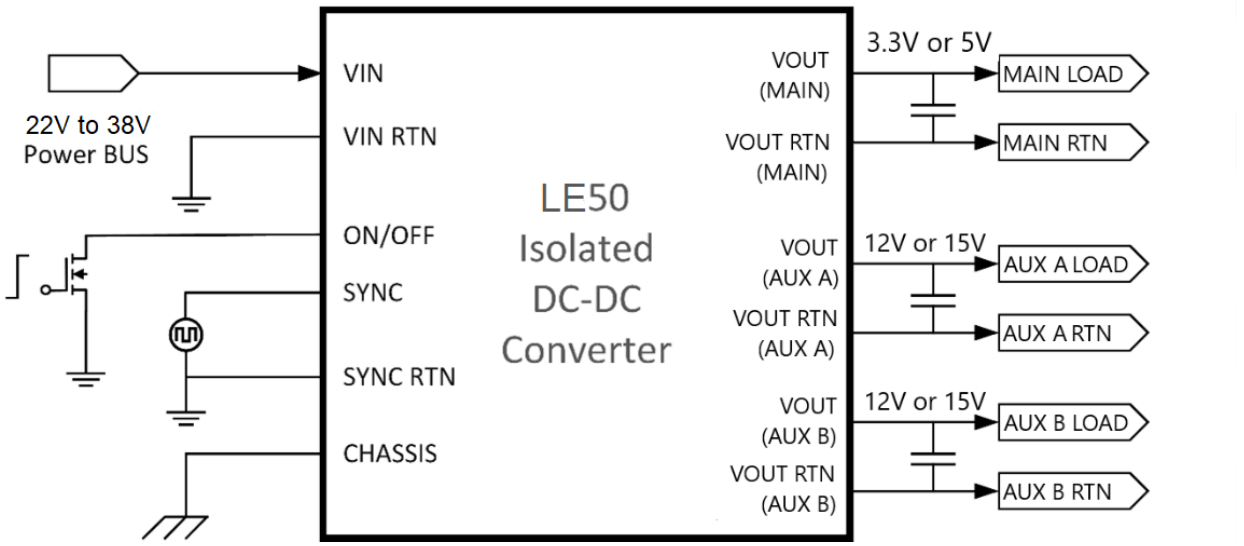
3. Typical Application Circuit

Figure 3-1. LE50-28T Single Typical Application Circuit

Figure 3-2.



LE50-28T AUX Outputs Parallel Application Circuit

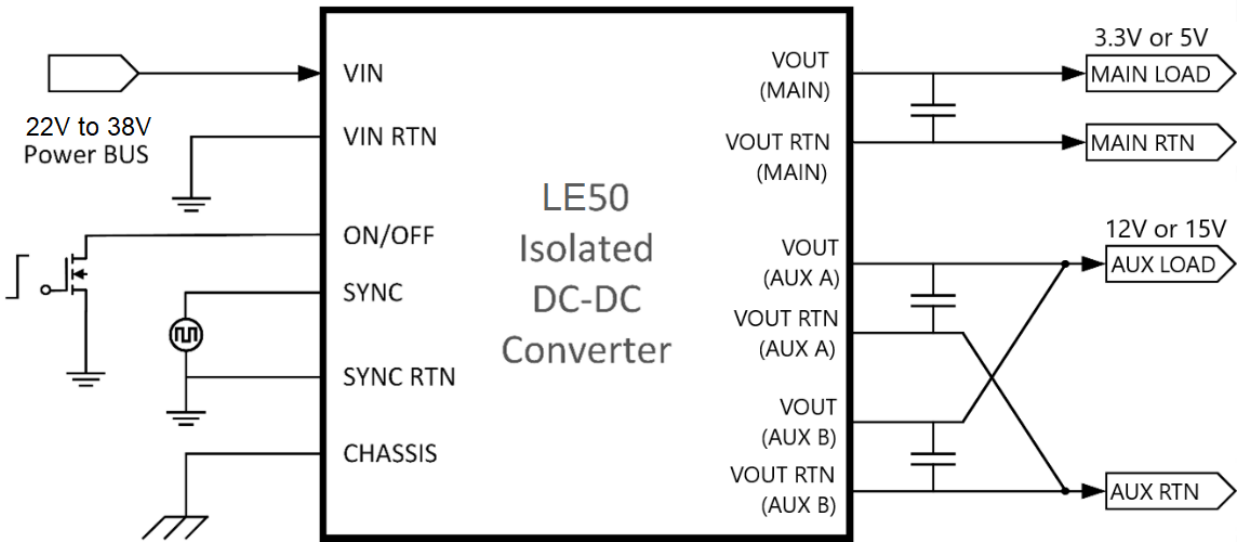


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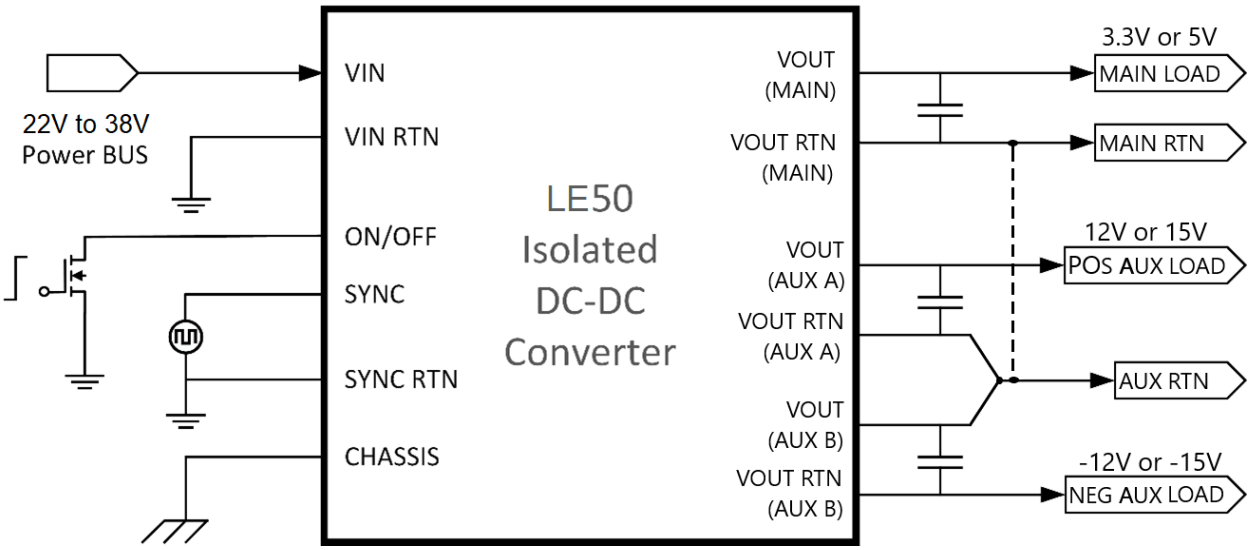
Figure 3-3. LE50-28T AUX Split Outputs Application Circuit



Note: With each output of the LE50 isolated from each other, there are more possible connections. These are circuits that will be found in typical applications.

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4. Absolute Maximum Ratings

Table 4-1. Absolute Maximum Ratings

Rating	Value
V_{IN} range	-0.5 VDC to 60 VDC
Output power	50W
Lead temperature	300 °C for 10s
Operating temperature	-55 °C to 70 °C
Storage temperature	-55 °C to 125 °C
Shock	1500 gpk, 0.5 ms, ½ sine
Constant acceleration	50g
Random vibration	24.06 grms, 50 Hz to 2000 Hz

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5. Electrical Parameters

This section shows the electrical parameters of the LE50-28 Triple Series device under the following conditions unless otherwise specified:

Table 5-1. Electrical Parameters

Parameter	Output	Conditions	Min	Nom	Max	Units
Input voltage all configurations						
(Vin)	—	Note 2	22	28	38	V
Output Voltages by configuration (V_{out})						
LE50-28-3R3-12T-x-x		I_{OUT} = 100% rated load				V
(MAIN)	3.3V		3.27	3.30	3.33	
(AUX A/B)	12V		11.59	12.00	12.41	
LE50-28-3R3-15T-x-x						
(MAIN)	3.3V		3.27	3.30	3.33	
(AUX A/B)	15V		14.25	14.75	15.25	
LE50-28-5-12T-x-x						
(MAIN)	5V		5.08	5.10	5.12	
(AUX A/B)	12V		11.75	12.00	12.24	
LE50-28-5-15T-x-x						
(MAIN)	5V		5.08	5.10	5.12	
(AUX A/B)	15V		14.25	14.75	15.25	
Output Power by configuration (P_{out})						
LE50-28-3R3-12T-x-x		Note 12	4.32	—	43	W
LE50-28-3R3-15T-x-x			4.32	—	43	
LE50-28-5-12T-x-x			5.0	—	50	
LE50-28-5-15T-x-x			5.0	—	50	

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Parameter	Output	Conditions	Min	Nom	Max	Units
Output current by configuration (I_{out})						
LE50-28-3R3-12T-x-x		In all cases, output power must be kept within P_{out} rating. Note 12, 13, 14, 15				mA
(MAIN)	3.3V		400	—	4000	
(AUX A/B)	12V		125	—	1250	
LE50-28-3R3-15T-x-x						
(MAIN)	3.3V		400	—	4000	
(AUX A/B)	15V		100	—	1000	
LE50-28-5-12T-x-x						
(MAIN)	5V		400	—	4000	
(AUX A/B)	12V		125	—	1250	
LE50-28-5-15T-x-x						
(MAIN)	5V		400	—	4000	
(AUX A/B)	15V		100	—	1000	
Line regulation by configuration (VR_{LINE})						
LE50-28-3R3-12T-x-x		V_{IN} = 22V, 28V, 38V I_{OUT} = 100% rated Note 11				mV
(MAIN)	3.3V		-20	—	20	
(AUX A/B)	12V		-120	—	120	
LE50-28-3R3-15T-x-x						
(MAIN)	3.3V		-20	—	20	
(AUX A/B)	15V		-150	—	150	
LE50-28-5-12T-x-x						
(MAIN)	5V		-20	—	20	
(AUX A/B)	12V		-120	—	120	
LE50-28-5-15T-x-x						
(MAIN)	5V		-20	—	20	
(AUX A/B)	15V		-150	—	150	

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Parameter	Output	Conditions	Min	Nom	Max	Units
Load regulation by configuration (VR_{LOAD})						
LE50-28-3R3-12T-x-x		V_{IN} = 28V I_{OUT} = 10%, 100% rated Note 10				mV
(MAIN)	3.3V		-50	—	50	
(AUX A/B)	12V		-400	—	400	
LE50-28-3R3-15T-x-x						
(MAIN)	3.3V		-50	—	50	
(AUX A/B)	15V		-500	—	500	
LE50-28-5-12T-x-x						
(MAIN)	5V		-50	—	50	
(AUX A/B)	12V		-400	—	400	
LE50-28-5-15T-x-x						
(MAIN)	5V		-50	—	50	
(AUX A/B)	15V		-500	—	500	
Cross regulation (VR_{cross})						
(Aux)	—	V_{IN} = 20V, 28V, 40V I_{OUT} = 2.5A to 1A and 2.5A to 4A on main, and ±half the rated current on the Aux outputs	-3.0	—	3.0	%
Input current all configurations (I_{IN})						
(Iin)	—	I_{OUT}=0, pin3 open	—	100	150	mA
		Pin 3 short to pin 2		2	5	
Output ripple all configurations (V_{RIP})						
(Main)	—	V_{IN} = 28V I_{OUT} = 100% rated, Note 3	—	25	50	mVpp
(Aux)	—		—	37.5	75	
Switching frequency all configurations (FS)						
(FS)	—	Sync input (pin 4) open	200	220	240	kHz
Efficiency by configuration (eff)						
LE50-28-3R3-12T-x-x		I_{OUT} = 100% rated load	75	82	—	%
LE50-28-3R3-15T-x-x			75	82	—	
LE50-28-5-12T-x-x			80	82	—	
LE50-28-5-15T-x-x			80	82	—	

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Parameter	Output	Conditions	Min	Nom	Max	Units
Inhibit input all configurations						
Inhibit input: ON Threshold		Note 1	4.5	—	—	V
Inhibit input: OFF (sink)			1000	—	—	µA
Inhibit input: OFF threshold			—	—	2	V
Current limit all configurations						
Current limit point (% rated output)		When V_{OUT} = 90% of nominal set point	105	—	145	%
Synchronization all configurations						
Synchronization frequency range		The external clock on sync input (pin 4) Note 1	500	—	600	kHz
Synchronization pulse-high level			4.0	—	10.0	V
Synchronization pulse-low level			–0.5	—	0.5	V
Synchronization pulse-transition rate			200	—	—	V/µs
Synchronization pulse-duty cycle			10	—	80	%
Power dissipation all conditions, load fault						
(P_D)	—	Short circuit, overload, Note 5	—	—	22	W
Output response to step load changes all configurations						
(V_{TLD})	—	(50% to/from 100%) rated load Note 6	-300	—	300	mVpk
Recovery time, step load changes all configurations						
(T_{TLD})	—	(50% to/from 100%) rated load Notes 6, 7	—	200	2000	µs
Output response to step line changes all configurations						
(V_{TLN})	—	20V to / from 40V I_{OUT} = 100% rated load Note 8	–300	—	300	mVpk
Recovery time, step line changes all configurations						
(T_{TLN})	—	20V to/from 40V I_{OUT} = 100% rated load Notes 7, 8	—	50	2000	µs

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Parameter	Output	Conditions	Min	Nom	Max	Units
Turn-on response: overshoot by configuration (V_{OS}) (main)						
LE50-28-3R3-12T-x-x		(0% to 100%) rated load Notes 4, 9				mV
(MAIN)	3.3V		—	—	500	
(AUX A/B)	12V		—	—	750	
LE50-28-3R3-15T-x-x						
(MAIN)	3.3V		—	—	500	
(AUX A/B)	15V		—	—	750	
LE50-28-5-12T-x-x						
(MAIN)	5V		—	—	500	
(AUX A/B)	12V		—	—	750	
LE50-28-5-15T-x-x						
(MAIN)	5V		—	—	500	
(AUX A/B)	15V		—	—	750	
Turn-on response: turn-on delay all configurations						
(T_{DLY})	—	Note 9	0.1	—	10	ms
Capacitive load by configuration (C_{LOAD})						
LE50-28-3R3-12T-x-x		Note 4				µF
(MAIN)	3.3V		—	—	1000	
(AUX A/B)	12V		—	—	250	
LE50-28-3R3-15T-x-x						
(MAIN)	3.3V		—	—	1000	
(AUX A/B)	15V		—	—	200	
LE50-28-5-12T-x-x						
(MAIN)	5V		—	—	1000	
(AUX A/B)	12V		—	—	250	
LE50-28-5-15T-x-x						
(MAIN)	5V		—	—	1000	
(AUX A/B)	15V		—	—	200	
Line rejection						
—	—	DC to 50 kHz, I_{OUT} = 100% rated load	40	60	—	dB

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.....continued						
Parameter	**Output**	**Conditions**	**Min**	**Nom**	**Max**	**Units**
Insulation resistance						
—	—	50V @25 °C 1. Input (1-3) to All (4-12) 2. Sync (4-5) to All (1-3, 6-12) 3. Chassis (6) to All (1-5, 7-12)	100	—	—	MΩ
Mass						
—	—	Standard case style A, B	—	120	—	g
MTBF						
—	—	MIL-HDBK-217F2, SF, 35°C	—	$1x10^6$	—	hrs
Isolation voltage						
—	—	—	—	100	—	V

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6. Radiation Specification

Table 6-1. Radiation Specification

Environment	Conditions	Min	Unit
TID (gamma)	MIL-STD-883, method 1019 The operating bias applied during exposure	50	krad (Si)
SEE/SEU, SEL, SEGR, SEB	Heavy ions [LET] The operating bias applied during exposure	37	MeV•cm^2/mg

Notes:

1. Parameter not 100% tested, and only assured by design.
2. Parameter verified during line and load regulation tests. Regulation is specified for 10% to 100% loading on all outputs.
3. Tested and verified using a 20 kHz to 10 MHz bandwidth. Ripple is measured across a 50 Ohms termination with a 10 nF Cap in series. Results applicable for DC to 20 MHz bandwidth.
4. The capacitive load may be any value from 0 to the maximum limit without compromising DC performance. A capacitive load exceeding the maximum limit may interfere with the proper operation of the converter's overload protection, potentially causing erratic behavior during turn-on.
5. Overload power dissipation is defined as the device power dissipation with the load set such that V_{OUT} = 90% of nominal.
6. The load step transition time is ≥ 10 µs.
7. Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within ±1% of its steady-state value.
8. The line step transition time is ≥ 100 µs.
9. Turn-on delay time from either a step application of input power or a logic low to a logic high transition on the inhibit pin (pin 3) to the point where V_{OUT} = 90% of nominal.
10. Load regulation relative to the output voltage at 50% rated load.
11. Line regulation relative to the output voltage at 28 VDC input.
12. For operation at temperatures between 70 °C and 100 °C, de-rate power linearly from 50W (or rated maximum) to zero. Parameter limits are not guaranteed.
13. Auxiliary output regulation is not maintained if main output load is less than 10%.
14. Auxiliary output requires at least 10% loading for specified regulation. Voltage may increase at lighter loads and is limited by overvoltage Zener diodes.
15. Unless otherwise specified, rated load means 20W on the main and 15W on each Auxiliary output. Other load settings are acceptable provided the total of 50W is not exceeded and minimum output current limits are satisfied.

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7. Sample Electrical Waveforms

These waveforms are for reference only.

Figure 7-1. LE50-28 Efficiency

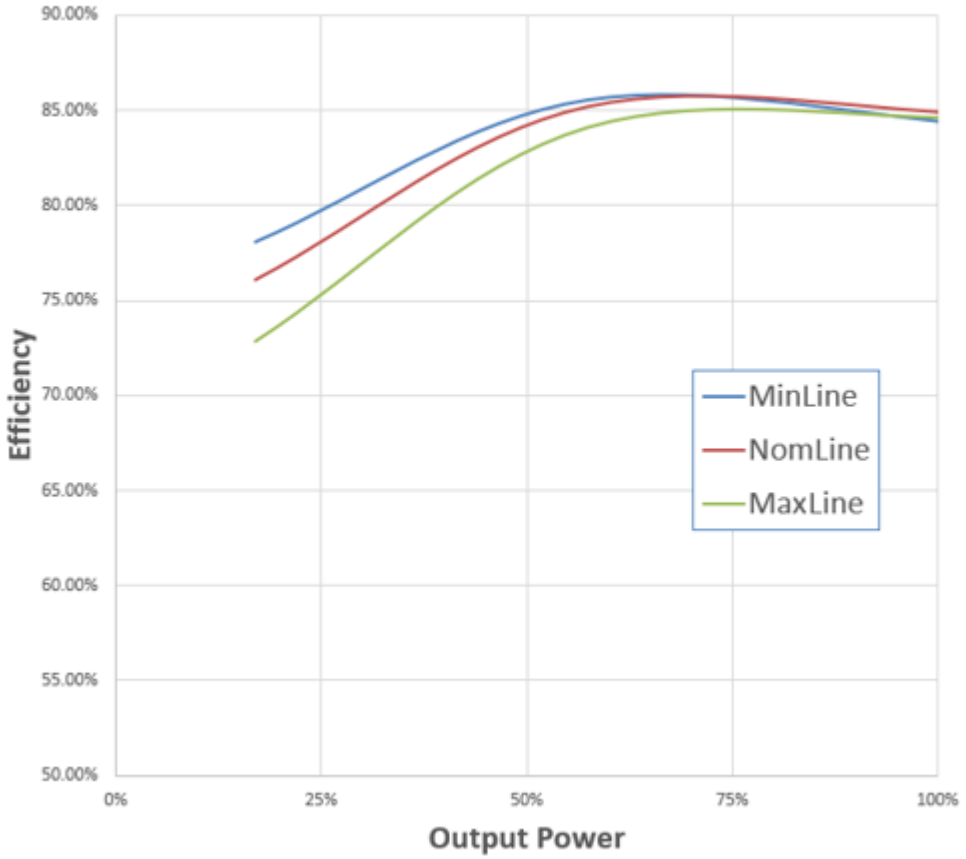

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Figure 7-2. LE50-28 EMI

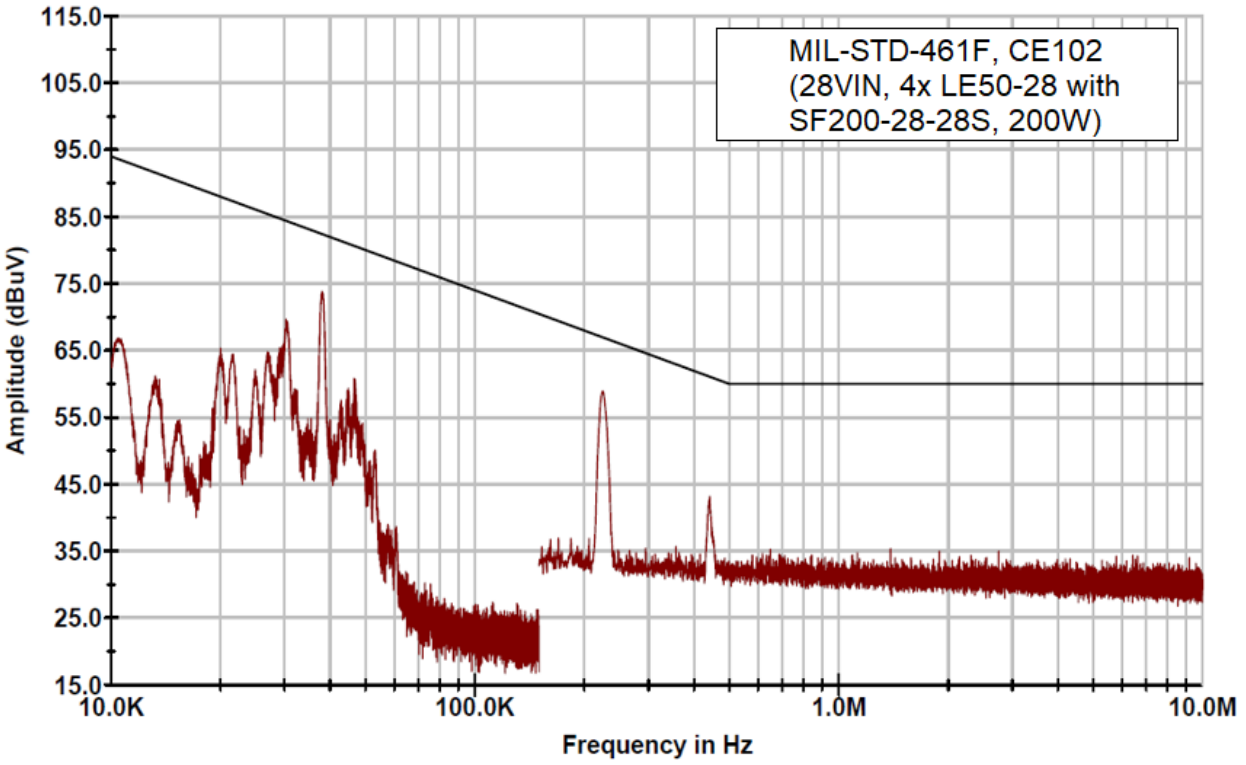

Figure 7-3. Typical Output Ripple

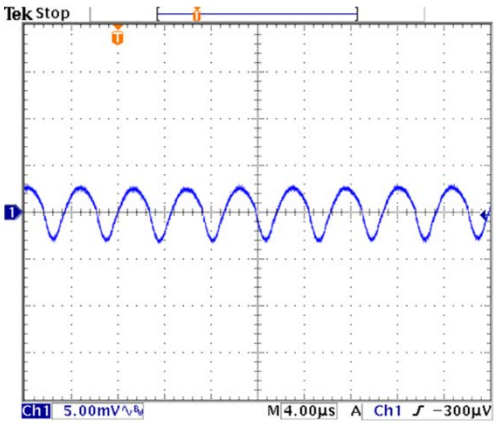

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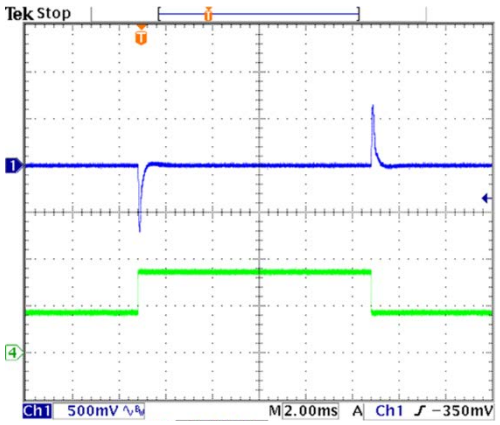
Figure 7-4. Typical 50% Load Step Transient Response



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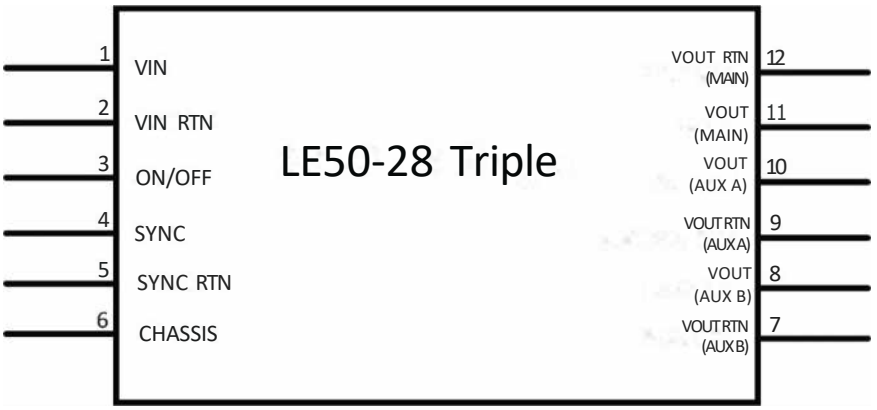
8. Pin Configuration

Figure 8-1. LE50-28 Triple Pin Configuration



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9. Pin Description

Table 9-1. Pin Description

PIN	NAME	Description
1	VIN	Input Voltage
2	VIN RTN	Input Voltage Return/Ground
3	ON/OFF (INHIBIT)	Power Supply ON/OFF, [ON(OPEN/HIGH), OFF(SHORT/LOW)]
4	SYNC	External Clock Signal Input
5	SYNC RTN	External Clock Signal Return
6	CHASSIS	Chassis Pin
7	VOUT (AUX B) RTN	Auxiliary B Vout return
8	VOUT (AUX B)	Auxiliary B Vout
9	VOUT (AUX A) RTN	Auxiliary A Vout return
10	VOUT (AUX A)	Auxiliary A Vout
11	VOUT (MAIN)	Main Vout
12	VOUT (MAIN) RTN	Main Vout return

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10. Radiation Performance (-T) Tolerant

- TID >50 krad (Si) and 30 krad (Si) ELDRS (<10 mrad/s) per MIL-STD-883 Method 1019
- SEE (SEGR, SEB, SET, SEL) immunity >37 MeV·cm^2/mg

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11. Mechanical Outline (Axial Pins) Package

Figure 11-1. Axial Pins and Through-hole Tabs Package (-A)

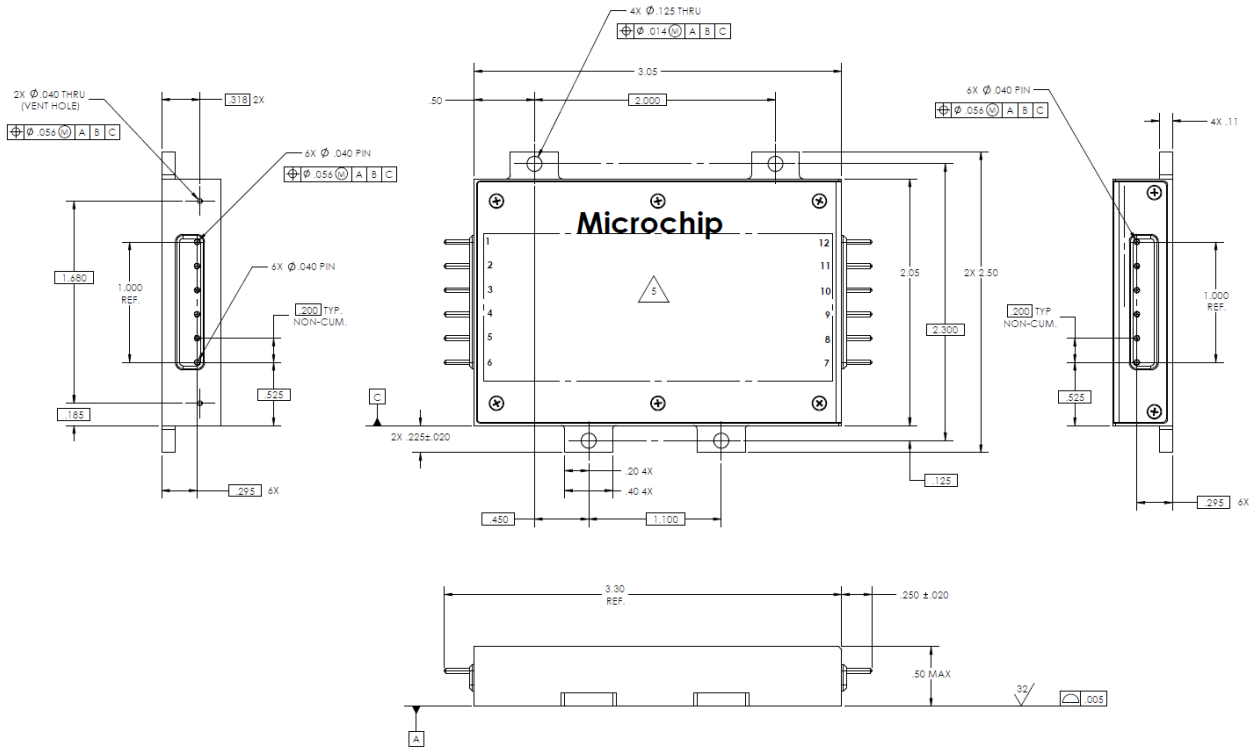
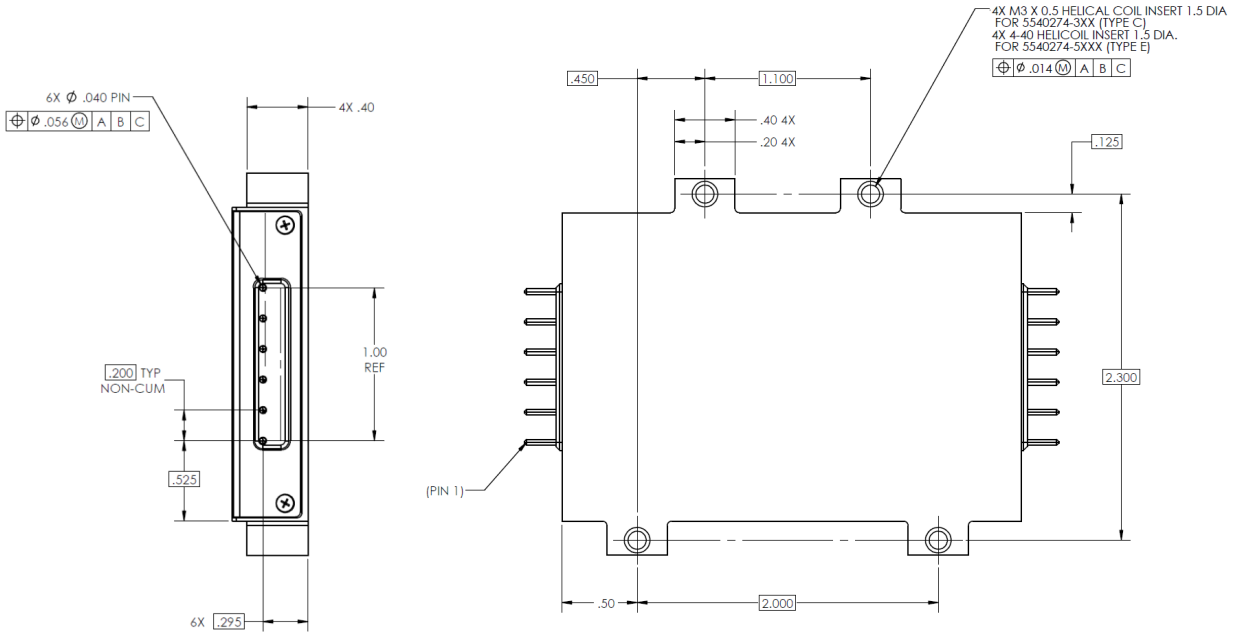


Figure 11-2. Axial Pins and Threaded Tabs Package Bottom View (-C or -E)



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12. Mechanical Outline (Radial Pins) Package

Figure 12-1. Radial Pins and Through-Hole Tabs Package (-D)

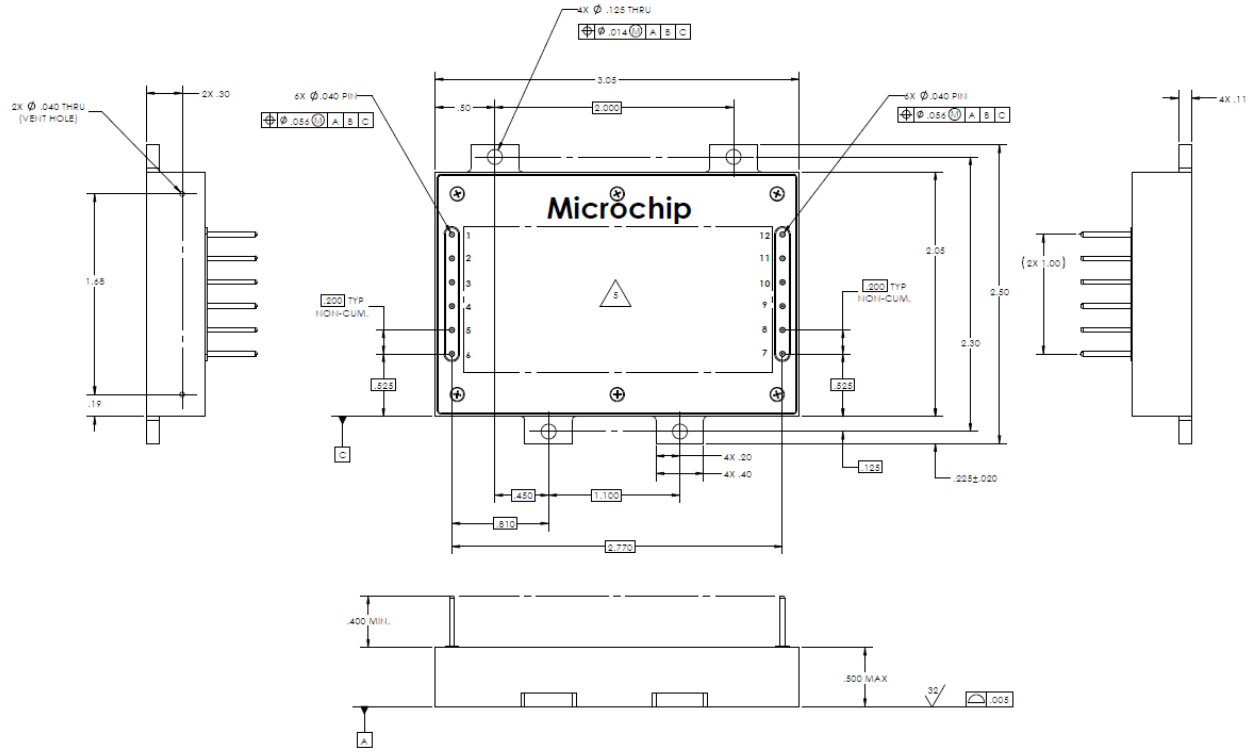
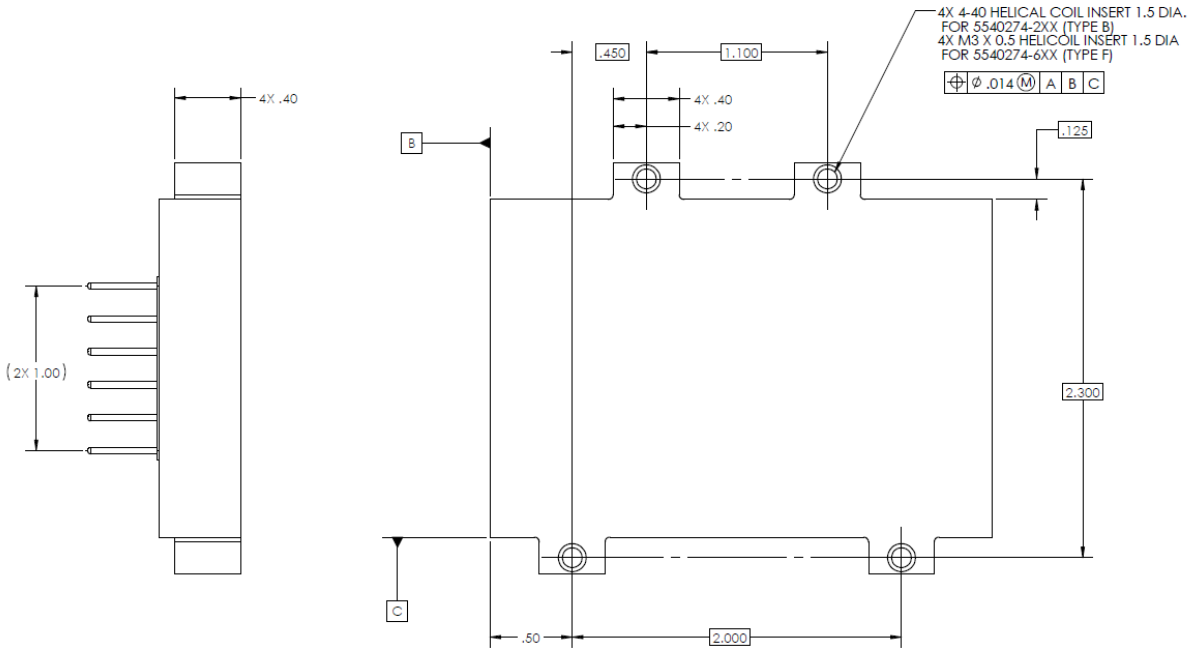


Figure 12-2. Axial Pins and Threaded Tabs Package Bottom View (-B or -F)



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13. Qualification Test

Table 13-1. Qualification Test

Test	Conditions
External Visual	Per O&M – Dimensions, and mass or MIL-STD-883, Method 2009
Electrical	Read and record (-55 °C, 25 °C, 70 °C)
Shock, Non-Operating	MIL-STD-202, method 213, test condition F, 1500 gpk, 0.5 ms ½ sine pulse. Three pulses in each direction of each axis, 18 pulses total.
Vibration, Operating	MIL-STD-202, method 214, condition II-F, 24.06 grms random vibrations, 50 Hz – 2000 Hz, 3 min/axis (9 min total). Outputs monitored.
Temperature Cycling	10 cycles from base plate temperature, MIL-STD-883, method 1010.9, condition C
EMI (with companion EMI filter)	CE101, CE102, CS101, RE101, RE102, RS101, RS103 per MIL-STD-461 with setup per MIL-STD-462.
External Visual Inspection	No damage
Steady State Life Test	1000 hrs at Tc = 85 °C, 50% of rated load
End-Point Electricals	Read and record (-55 °C, 25 °C, 70 °C)

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14. ATP Screening Test (-T) Tolerant

Table 14-1. ATP Screening Test (-T) Tolerant

Requirement	Test Method/Condition
External Visual	O&M – Dimensions and mass
Initial Electrical	Full performance at +25 °C
Vibration (Optional)	Workmanship non-operating vibration MIL-STD-202, Method 214, Condition II-A, 6.21 grms random vibration, 50-2000 Hz, 1-minute perpendicular to the board
Temperature Cycle (Optional)	MIL-STD-883, Method 1010, Condition A, 1 cycle, +70 °C to -55 °C, operating Outputs monitored during thermal cycles
Burn-in (at 25 °C or Optional)	40 Hrs @ 70 °C, 50% of rated load (outputs monitored)
Final Electrical (Optional)	Full performance at +25 °C (deliverable data)
External Visual	No damage

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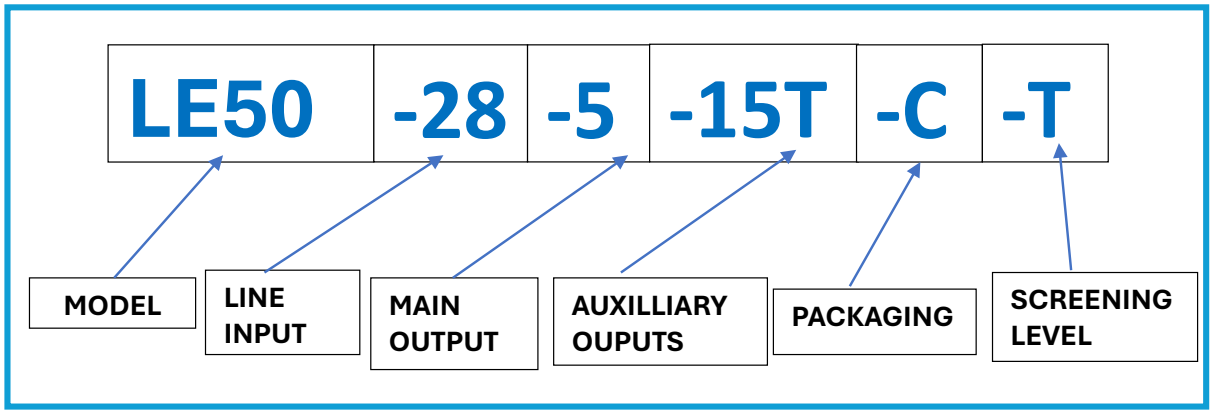
15. Ordering Information



Model	LE50	Standard Applications 50W, 28V input modules		
Line input	-28	28.0V	Line input voltage. Nominal input line	
Main	-3R3	3.3V	Main output voltage	
	-5	5.0V		
Aux	-12T	12.0V	Auxiliary output voltages (A and B outputs identical) (T is for triple)	
	-15T	15.0V		
Mechanical Package	-A	Axial	0.125 in through-hole	Mechanical packaging options. Electrical connections are either Radial or Axial. Mounting holes are drilled through-hole or Threaded.
	-B	Radial	4-40 thread	
	-C	Axial	M3 thread	
	-D	Radial	0.125 in through-hole	
	-E	Axial	4-40 thread	
	-F	Radial	M3 thread	
Radiation Tolerance	-T	Tolerant	—	

Note: Other input voltage and output voltage combinations are available. Contact your local sales representative.
Microchip also offers a thermal interface, the ST-2X3; this is a non-silicon, space-approved thermal interface. The data sheet is available upon request.

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16. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	04/2024	Initial Revision

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Microchip Information

The Microchip Website

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