DC–67 GHz GaAs MMIC Distributed Driver Amplifier

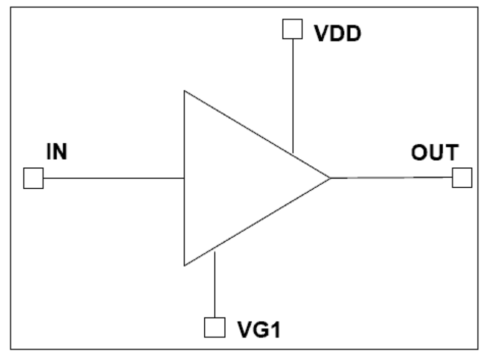
Product Overview

MMA121AA is a DC-67GHz, gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) pseudomorphic high-electron-mobility transistor (pHEMT) distributed amplifier. It is ideal for test instrumentation and wide-band A&D and space applications. The amplifier provides 13 dB of gain, 17dBm of P1dB at 50GHz and 13dBm at 65GHz with a nominal bias condition of 200 mA from a 7V supply. Output IP3 is typically 32 dBm at 35GHz. Die has an on-chip Bias network allowing smooth operation from 1 to > 67GHz. For operation below 1GHz an external choke network should be used. The MMA121AA amplifier is DC coupled and features RF I/Os that are internally matched to 50 Ω.

Key Features

- **Frequency range: DC to 67 GHz**
- **Gain: 13 dB**
- **High Power: 15dBm @ 65GHz**
- **Supply: 7 V at 200 mA**
- **Integrated On-chip Bias**
- **Handle high power input 20dBm**
- **50 Ω matched input/output**
- **Die size: 1.15 x 1.65 x 0.1 mm**

Functional Block Diagram



Applications

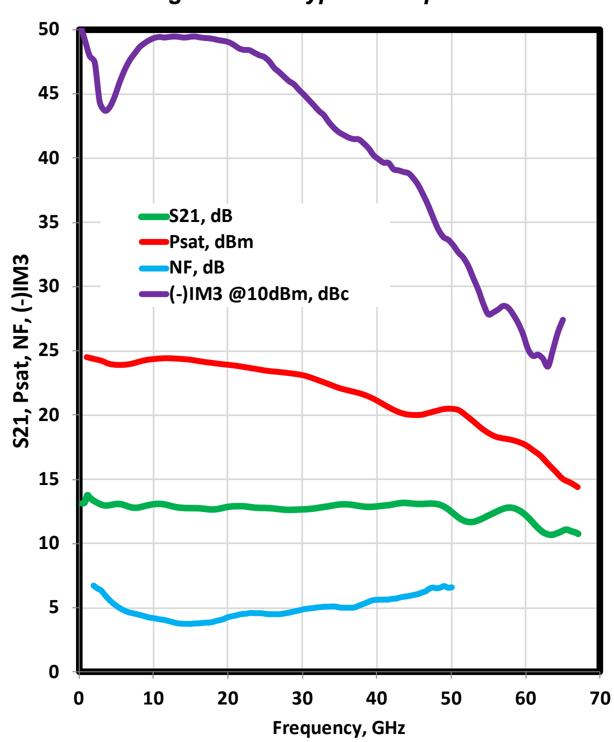
- Test and measurement instrumentation
- Electronic warfare (EW), electronic countermeasures (ECM), and electronic counter-countermeasures (ECCM)
- Military, A&D, space, SATCOM
- Telecom infrastructure
- Wideband microwave radios
- Microwave and millimeter-wave communications systems

Performance Overview

Parameter	Typ.	Units
Operational frequency range	DC-67	GHz
Gain	13	dB
Noise figure	4	dB
P1dB @ 50GHz	17	dBm
Psat @ 50GHz	20	dBm
IM3 @ 50 GHz and 10dBm	-33	dBc
Current @ +7V Supply	200	mA

Export Classification: **3A001.b.2.d**

Figure 1 - Typical Responses



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1. Electrical Specifications

1.1. Typical Electrical Performance

Table 1 - Typical Electrical Performance at 25 C, Vdd=7V, Idd=200 mA (Unless otherwise mentioned)

Parameter	Frequency Range	Min	Typ.	Max	Units
Frequency range		DC		67	GHz
Gain	DC–20 GHz	12	13		dB
	20 GHz–40 GHz	12	13		dB
	40GHz–67 GHz	12	13		dB
Gain flatness	DC–20 GHz		±1		dB
	20 GHz–40 GHz		±1		dB
	40GHz–67 GHz		±1		dB
Noise figure	3–20 GHz		4	7	dB
	20 GHz–40 GHz		5	6	dB
Input return loss	DC–20 GHz	13	15		dB
	20 GHz–40 GHz	13	15		dB
	40GHz–67 GHz	8	12		dB
Output return loss	DC–20 GHz	11	15		dB
	20 GHz–40 GHz	10	13		dB
	40GHz–67 GHz	9	12		dB
P1dB	DC–20 GHz	20	22		dBm
	20 GHz–40 GHz	18	20		dBm
	40GHz–67 GHz	11	17		dBm
Psat	DC–20 GHz	22	24		dBm
	20 GHz–40 GHz	19	22		dBm
	40GHz–67 GHz	14	17		dBm
OIP3	DC–20 GHz	31	34		dBm
	20 GHz–40 GHz	29	32		dBm
	40GHz–67 GHz	20	26		dBm
VDD (drain voltage supply)			7		V
IDD (drain current)			200		mA

1.2. Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the MMA121AA device at 25 °C, unless otherwise specified. Exceeding one or any of the maximum ratings potentially could cause damage or latent defects to the device.

Table 2 - Absolute Maximum Ratings

Parameter	Rating
Drain bias voltage (V_{DD})	8 V
Gate bias voltage (V_G)	–2 V to 0.5 V
RF input power (Pin)	20 dBm
Channel temperature	165 °C
V_{DD} current (I_{DD})	300 mA
DC power dissipation (T = 85 °C)	1.7 W
Thermal resistance	47 °C/W
Storage temperature	–65 °C to 150 °C
Operating temperature	–55 °C to 85 °C

ESD Sensitive Device

1.3. Typical Performance Curves

1.3.1 Typical Performances vs. Temperature

The following graphs show the typical performance curves of the MMA121AA device at specific bias conditions, measurements performed using Test Circuit shown on Figure 55 -below.

Figure 2 - Gain vs. Temperature @ 6V/150mA

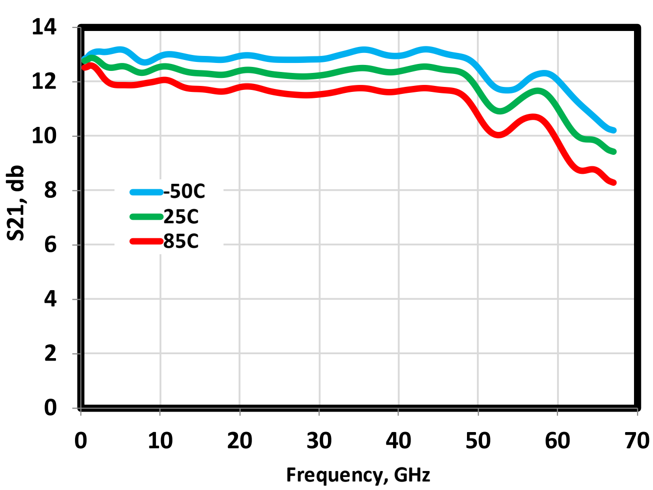


Figure 3 - Gain vs. Temperature @ 7V/200mA

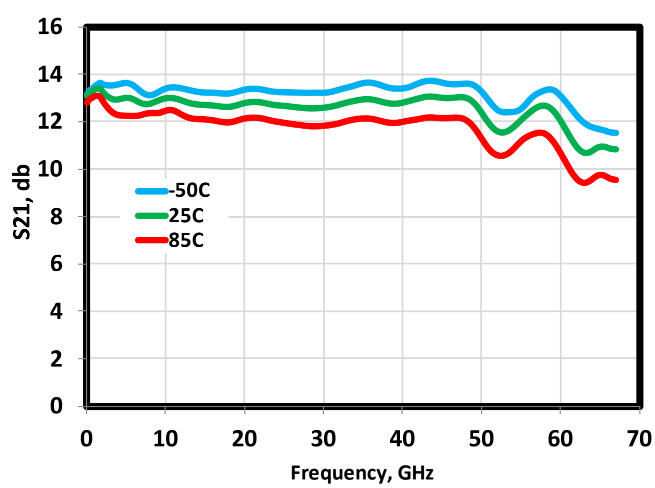


Figure 4 - Gain vs. Temperature @ 7.5V/250mA

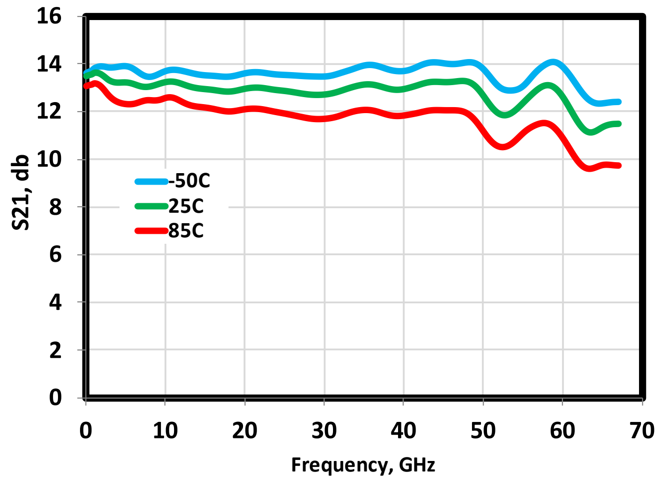


Figure 5 - Gain vs. Temperature @ 8V/300mA

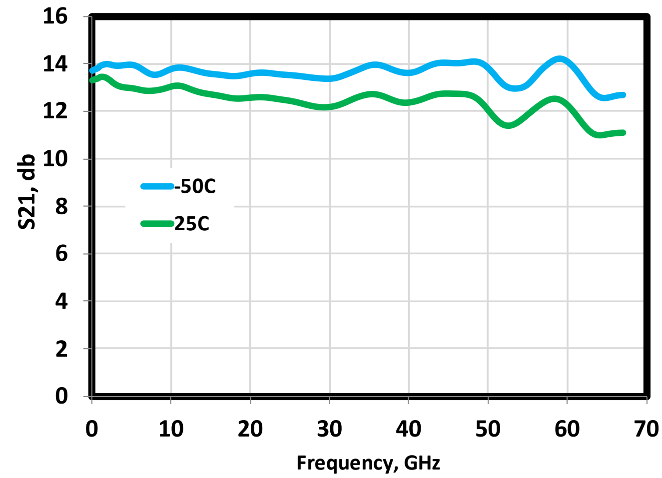


Figure 6 - S11 vs. Temperature @ 6V/150mA

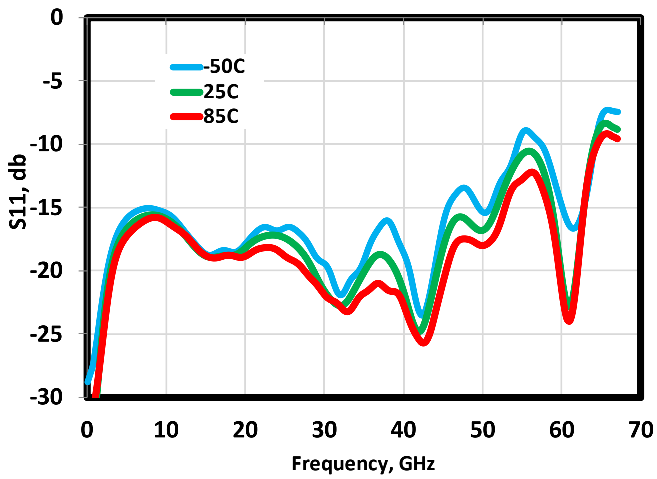


Figure 7 - S11 vs. Temperatu re @ 7V/200mA

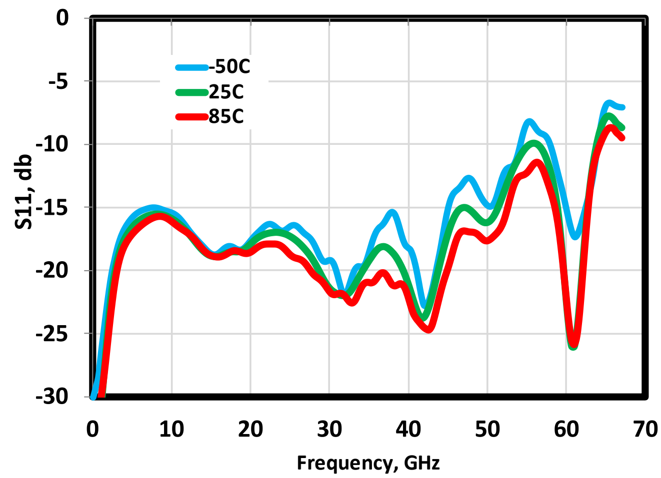


Figure 8 - S11 vs. Temperature @ 7.5V/250mA

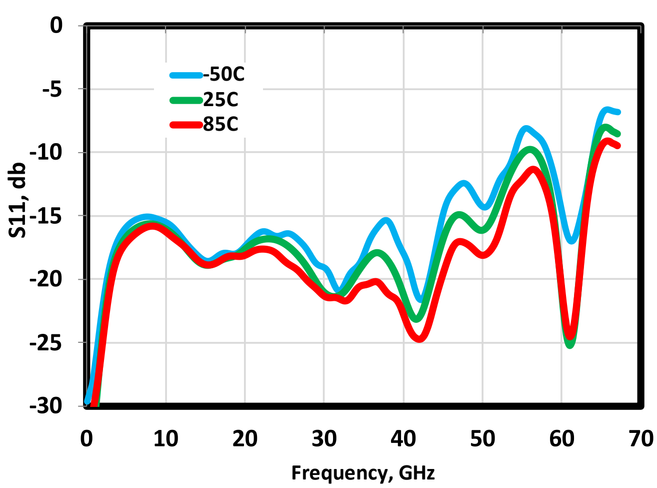


Figure 9 - S22 vs. Temperature @ 6V/150mA

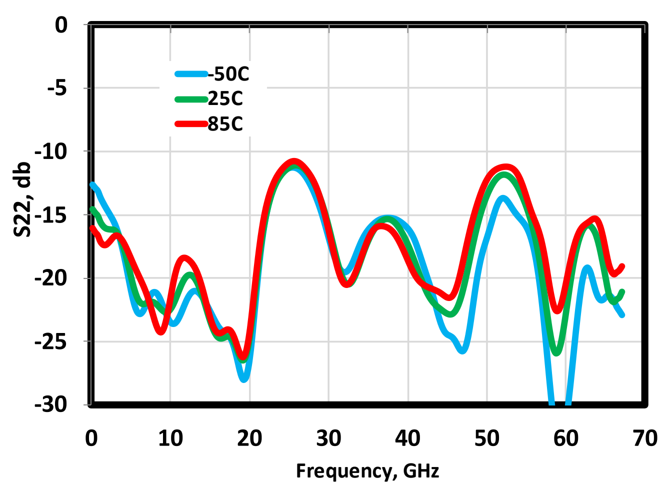


Figure 10 - S22 vs. Temperature @ 7V/200mA

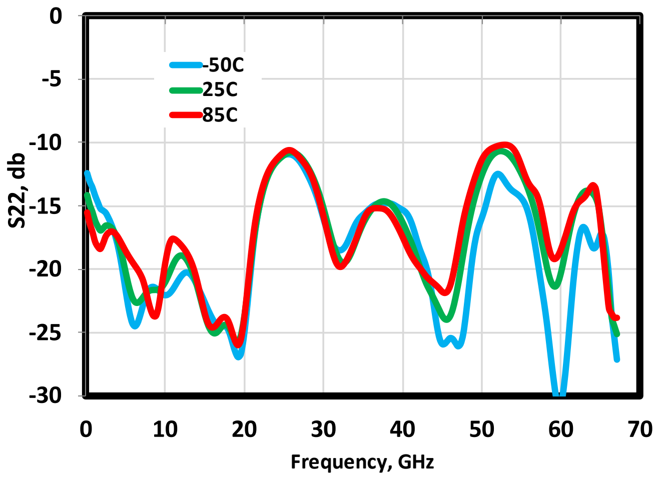


Figure 11 - S22 vs. Temperature @ 7.5V/250mA

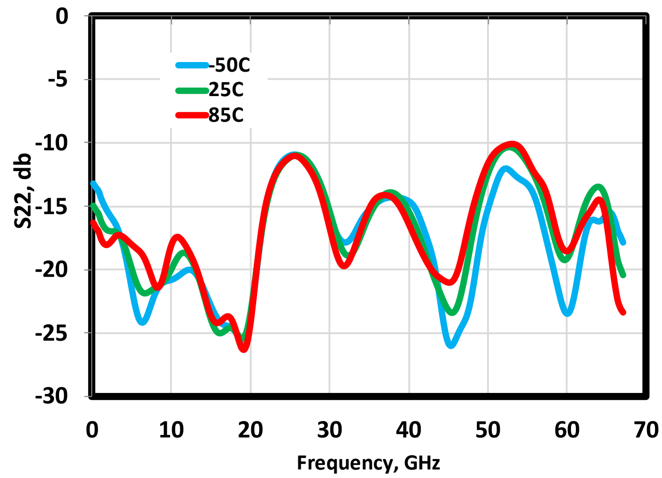


Figure 12 - S12 vs. Temperature @ 6V/150mA

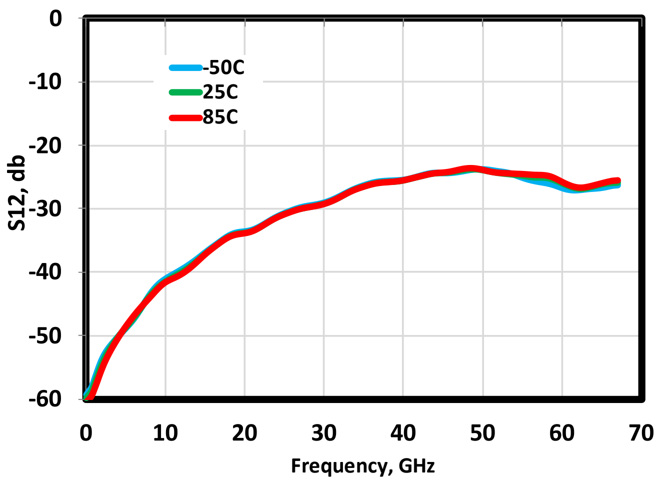


Figure 13 - S12 vs. Temperature @ 7.5V/250mA

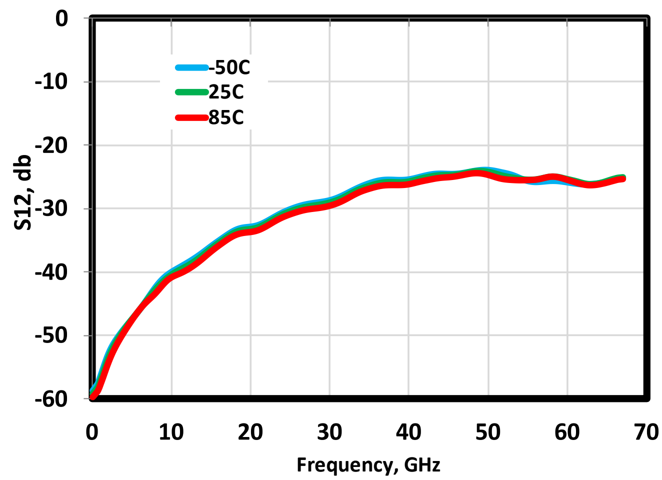


Figure 14 - NF vs. Temperature @ 6V/150mA

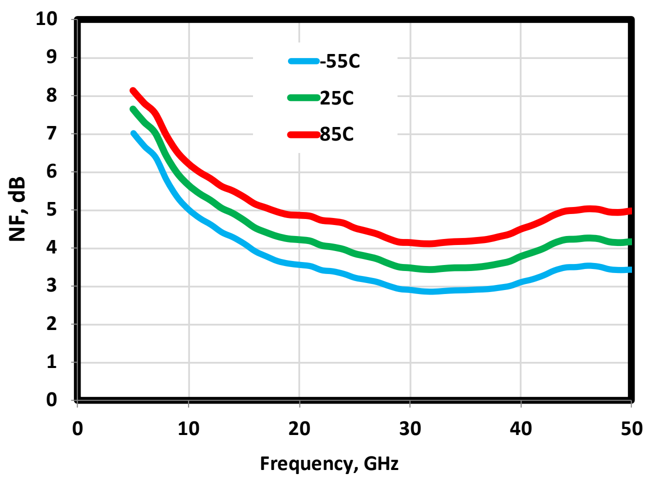


Figure 15 - NF vs. Temperature @ 7V/200mA

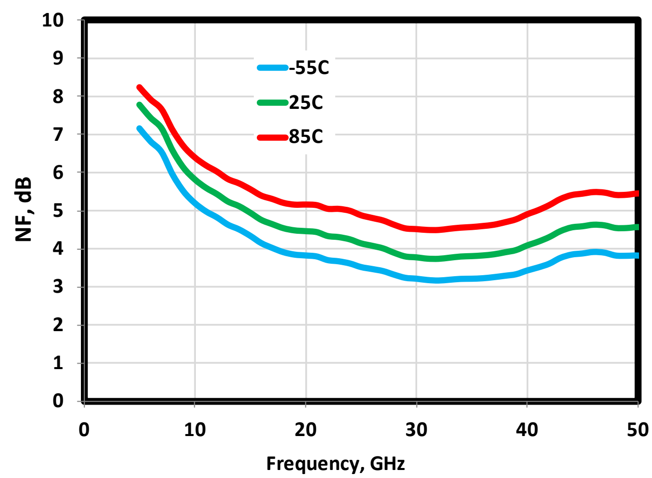


Figure 16 - NF vs. Temperature @ 7.5V/250mA

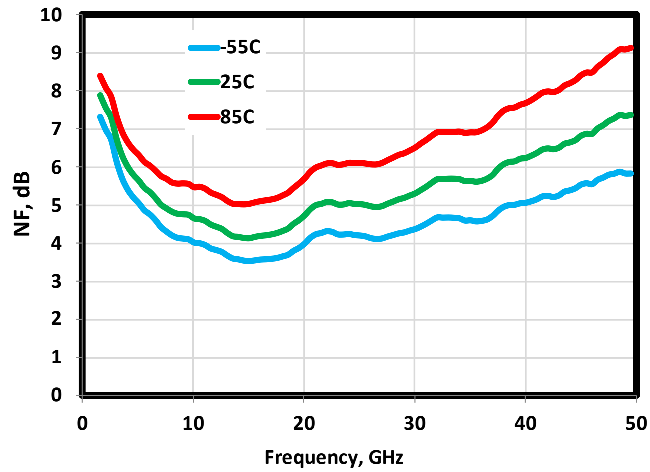


Figure 17 - P1dB vs. Temperature @ 6V/150mA

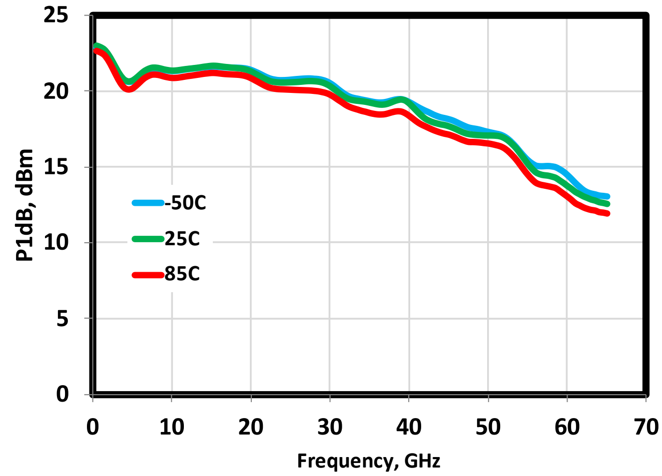


Figure 18 - P1dB vs. Temperature @ 7V/200mA

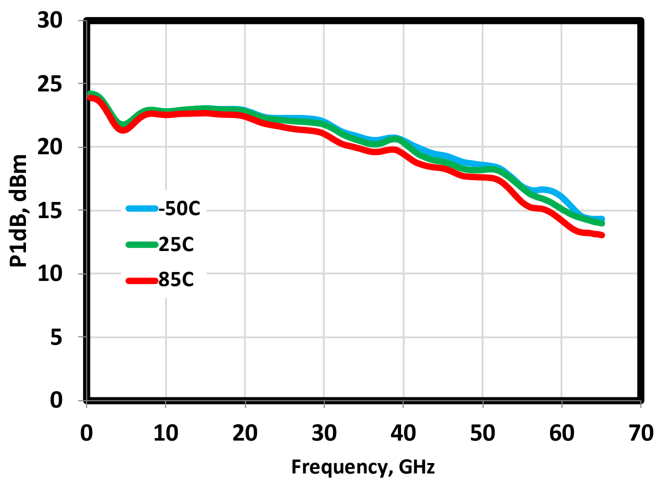


Figure 19 - P1dB vs. Temperature @ 7.5V/250mA

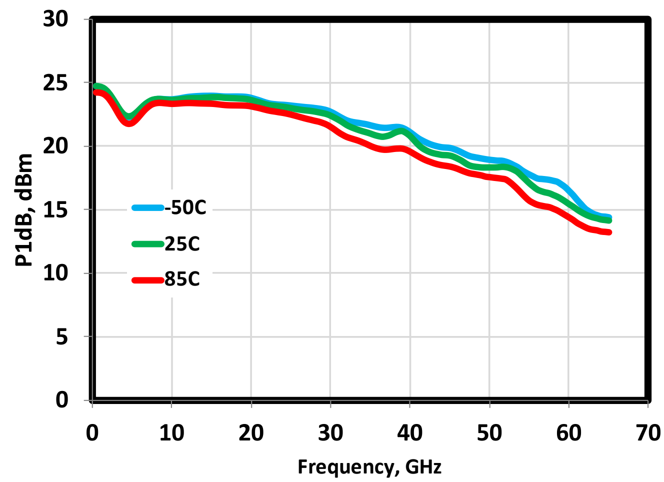


Figure 20 - Psat vs. Temperature @ 6V/150mA

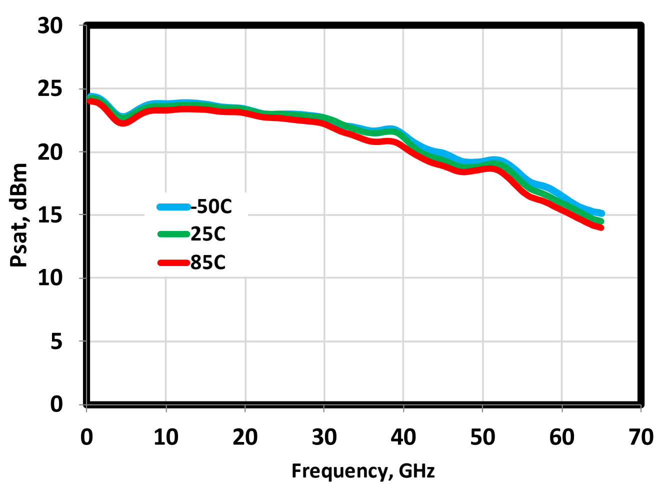


Figure 21 - Psat vs. Temperature @ 7V/200mA

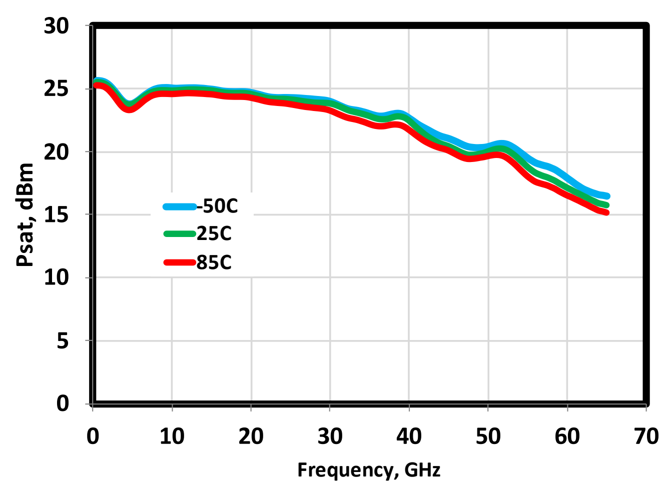


Figure 22 - Psat vs. Temperature @ 7.5V/250mA

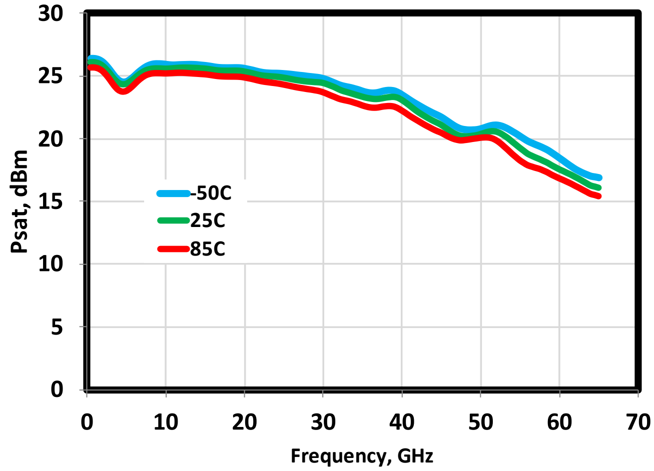


Figure 23 - IM2(low) vs. Temperature @ 6V/150mA at 10dBm per tone

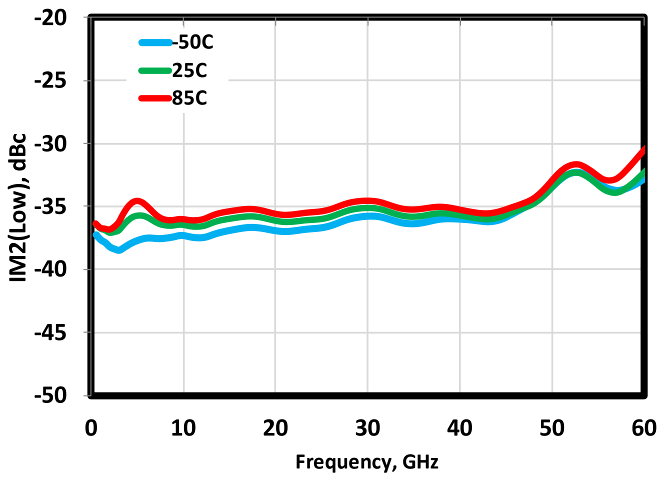


Figure 24 - IM2(low) vs. Temperature @ 7V/200mA at 10dBm per tone

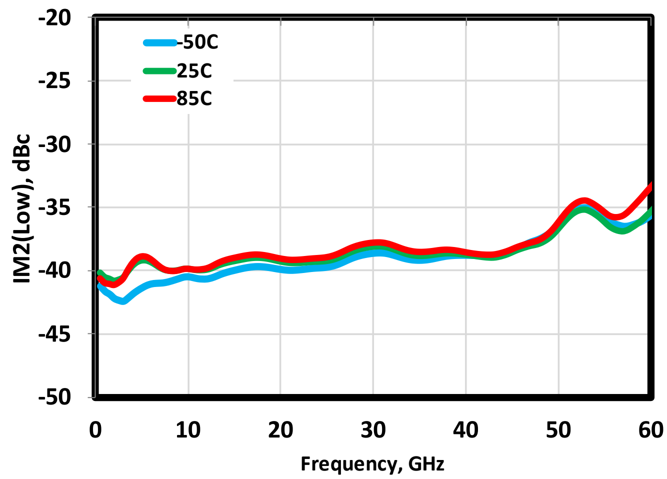


Figure 25 - IM2(low) vs. Temperature @ 8V/300mA at 10dBm per tone

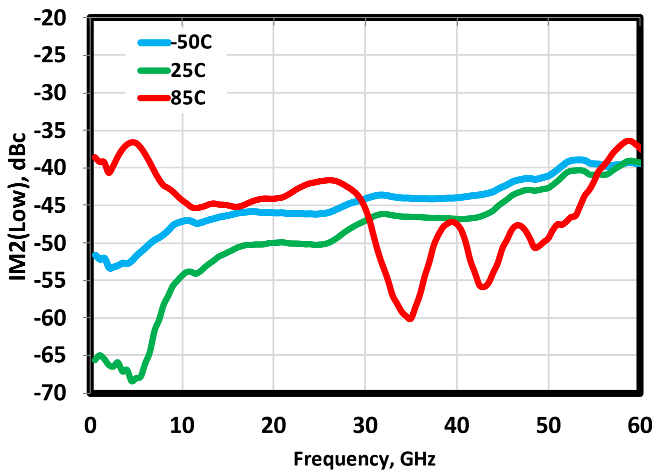


Figure 26 - IM3 vs. Temperature @ 6V/150mA, 10dBm(per tone)

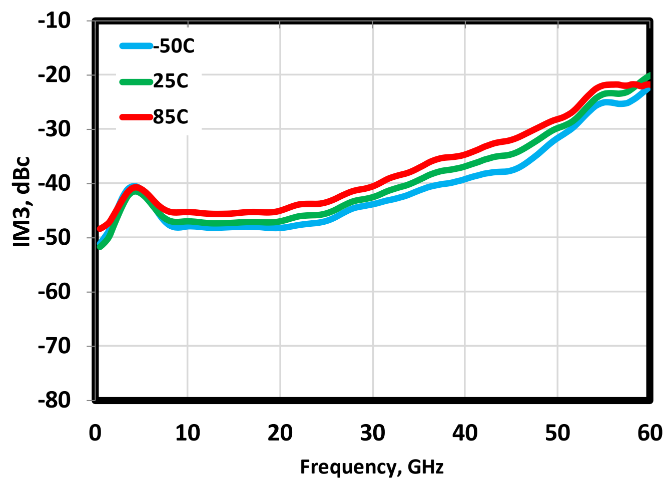


Figure 27 - IM3 vs. Temperature @ 7V/200mA, 10dBm(per tone)

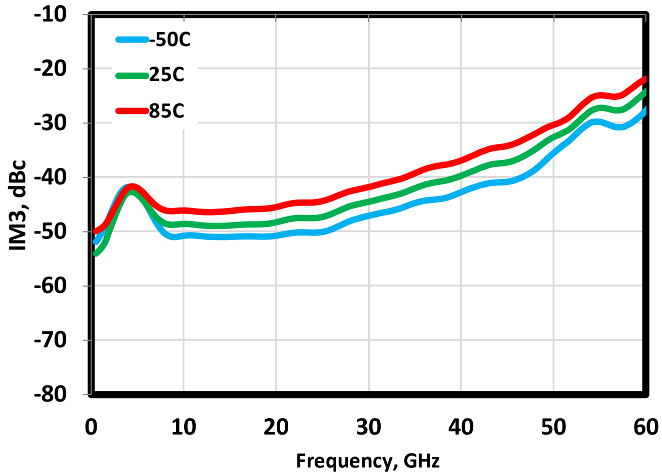
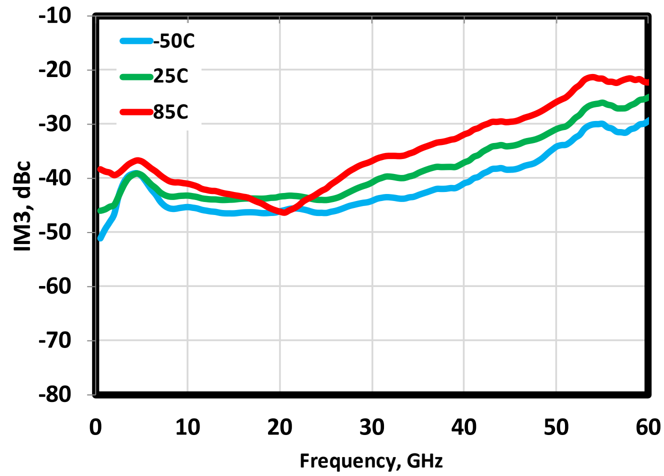


Figure 28 - IM3 vs. Temperature @ 8V/300mA, 10dBm(per tone)



1.3.2 Typical Performances vs. Bias

The following graphs show the typical performance curves of the MMA121AA device at 25 °C vs. Bias conditions, measurements performed using Test Circuit shown on Figure 55 -below.

Figure 29 - Gain vs . V_{DD} @ 150mA

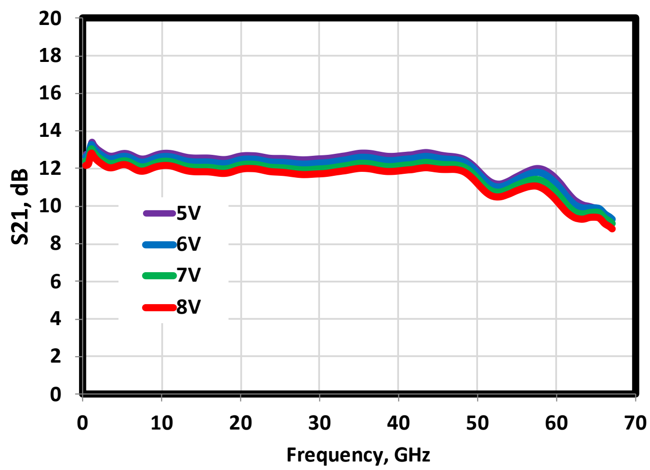


Figure 30 - Gain v s. V_{DD} @ 200mA

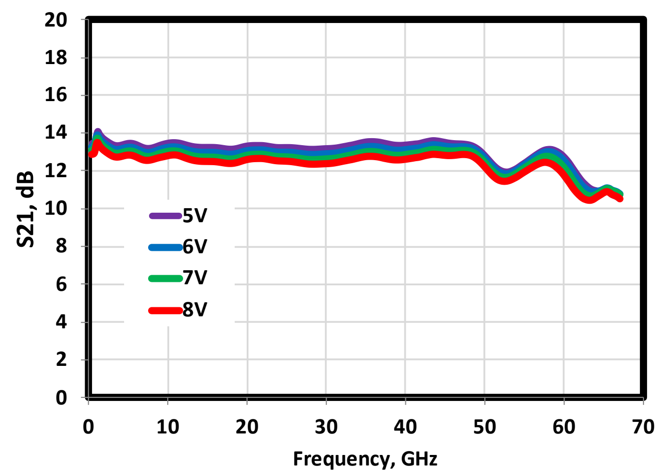


Figure 31 - Gain vs. V_{DD} @ 250mA

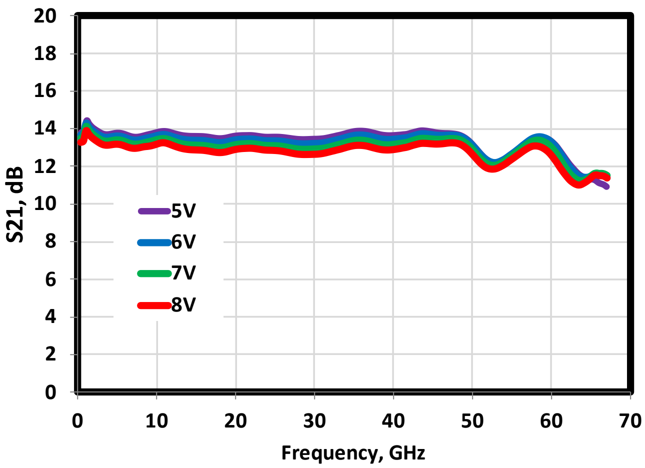


Figure 32 - Gain vs. V_{DD} @ 300mA

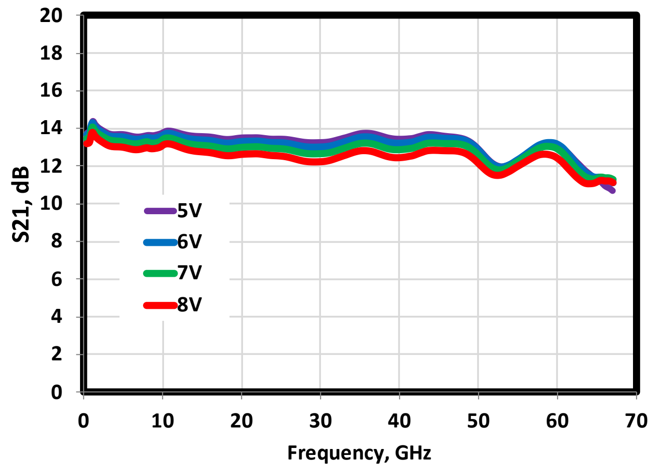


Figure 33 - NF vs. V_{DD} @ 150mA

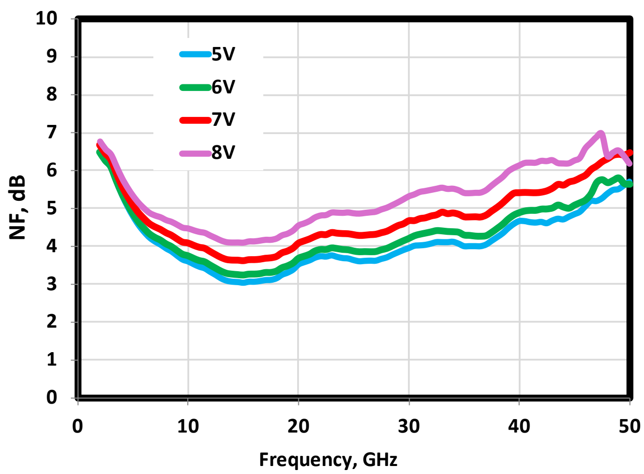


Figure 34 - NF vs. V_{DD} @ 200mA

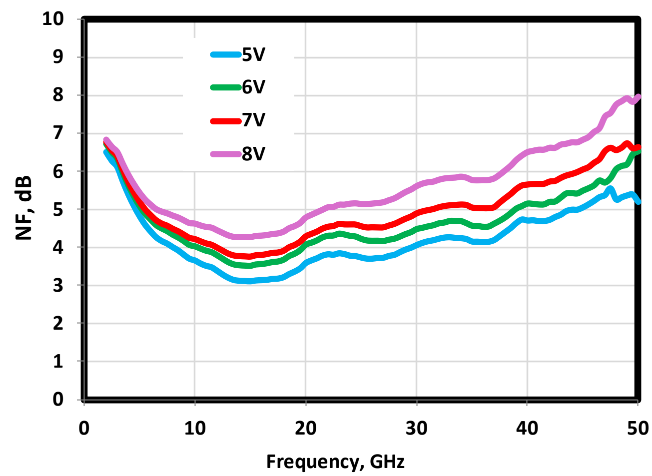


Figure 35 - NF vs. V_{DD} @ 250mA

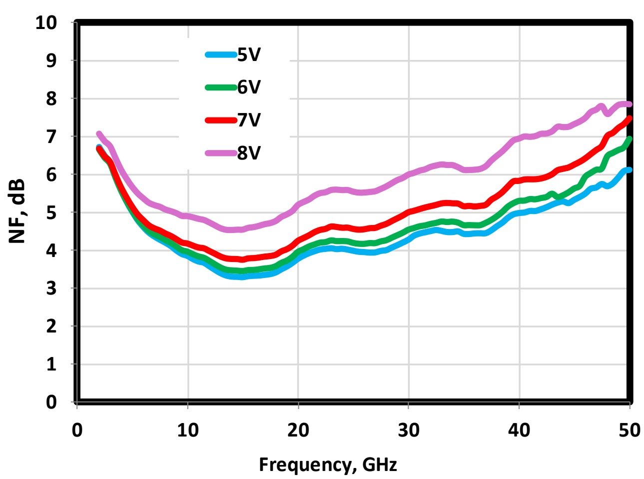


Figure 36 - NF vs. V_{DD} @ 300mA

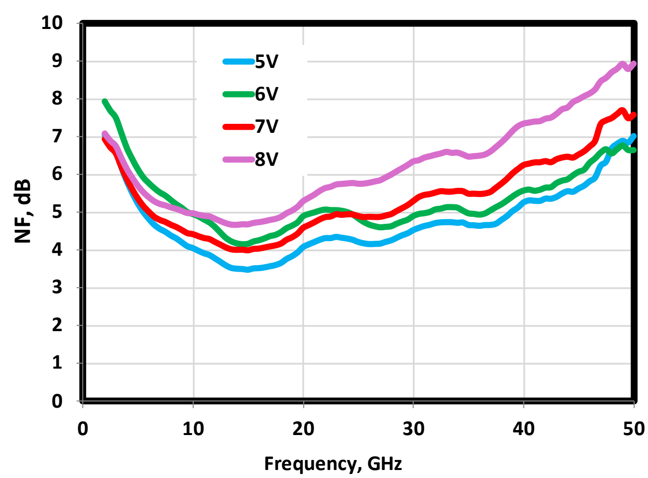


Figure 37 - P1dB Bias

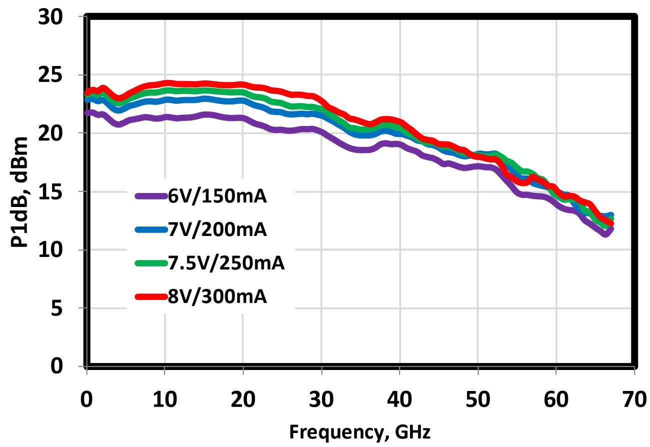


Figure 38 - Psat vs. Bias

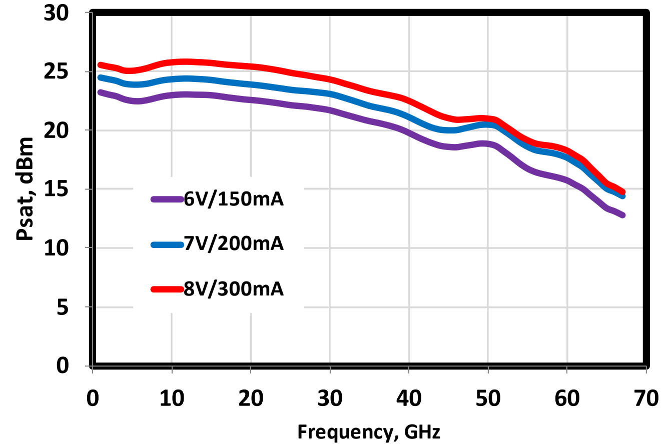


Figure 39 - OIP3 vs. Bias

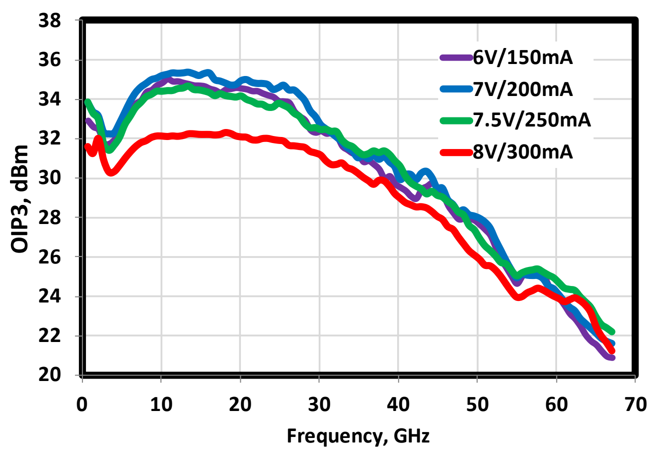


Figure 40 - IM3 vs. Bias at 10dBm per tone

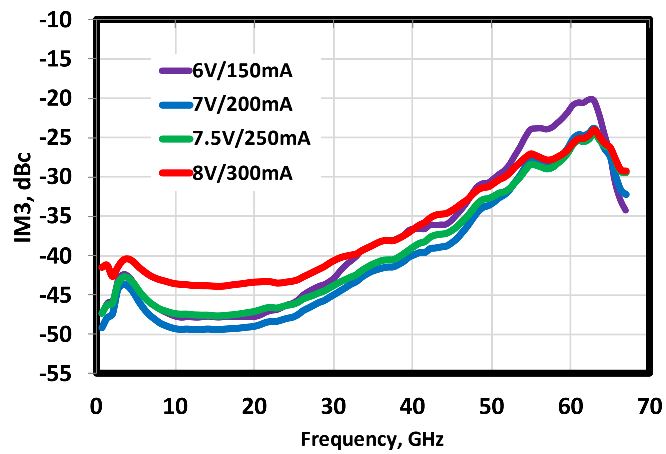
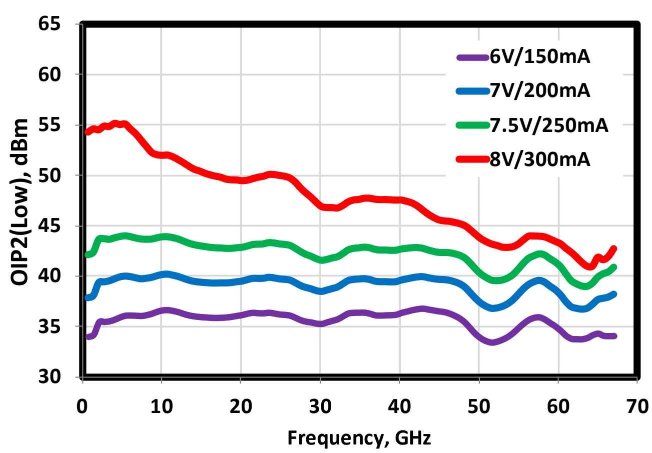


Figure 41 - OIP2 Low at Δ=10MHz) vs. Bias



1.3.3 Typical Performances vs. Output Power

The following graphs show the typical performance curves of the MMA121AA device at 25 °C vs. Output Power conditions, measurements performed using Test Circuit shown on Figure 55 -below.

Figure 42 - IM2 vs. Power @ 6V/150mA

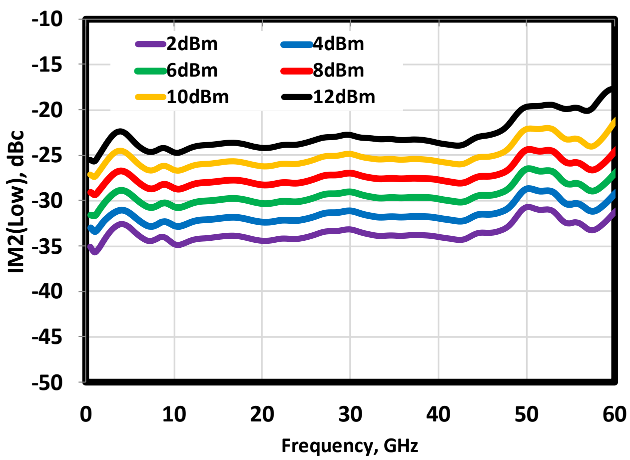


Figure 43 - IM2 vs. Power @ 7V/200mA

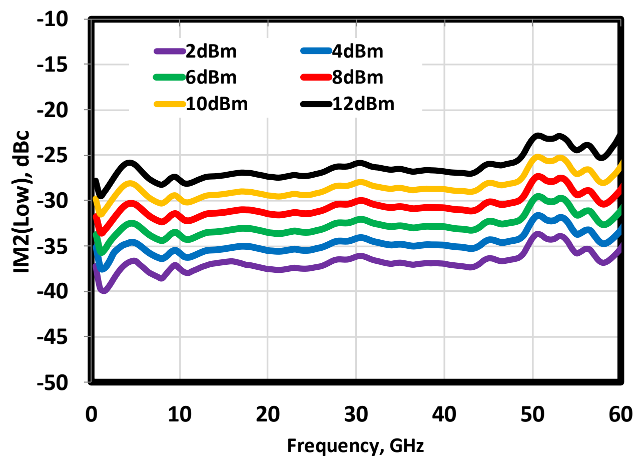


Figure 44 - IM2 vs. Power @ 7.5V/250mA

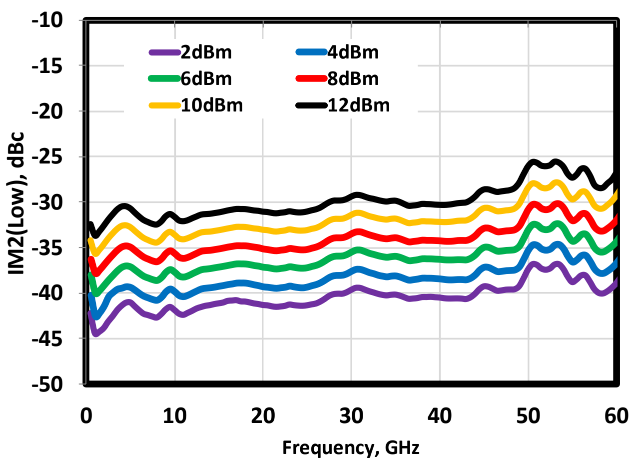


Figure 45 - IM2 vs. Power @ 8V/250mA

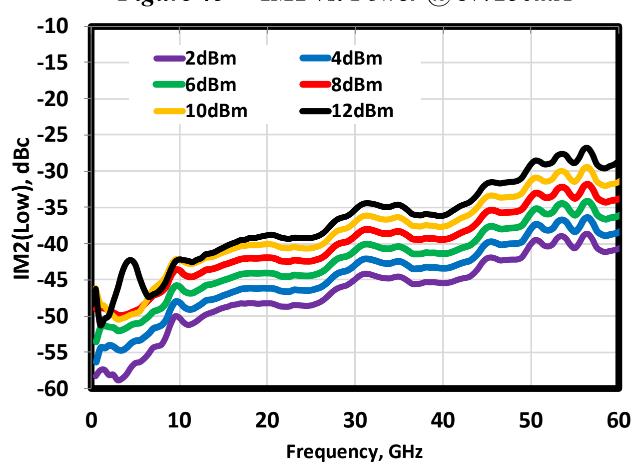


Figure 46 - IM3 vs. Power @ 6V/150mA

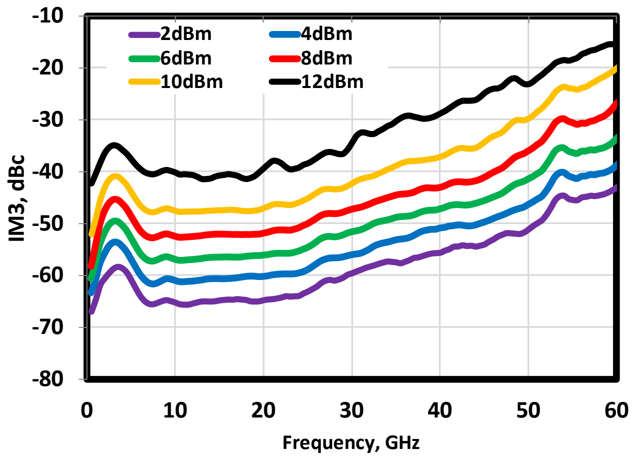


Figure 47 - IM3 vs. Power @ 7V/200mA

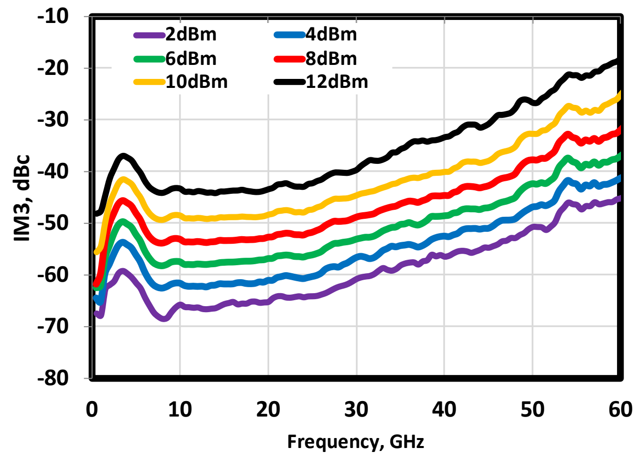


Figure 48 - IM3 vs. Power @ 7.5V/250mA

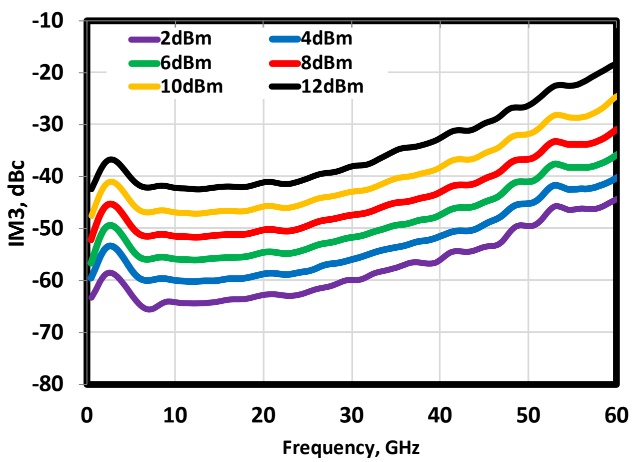


Figure 49 - IM3 vs. Power @ 8V/250mA

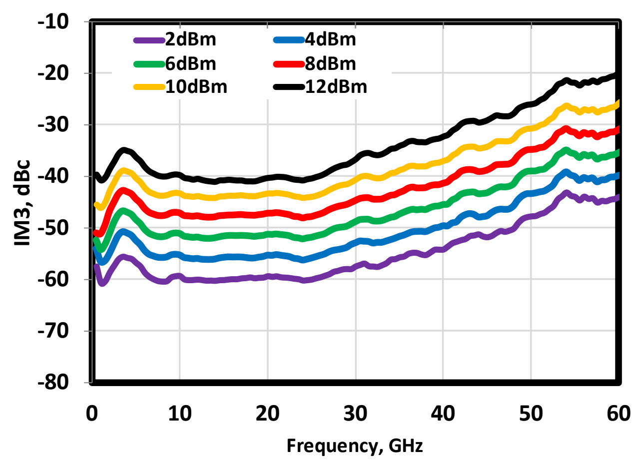


Figure 50 - 2-nd Harmonic vs. Power @ 6V/150mA

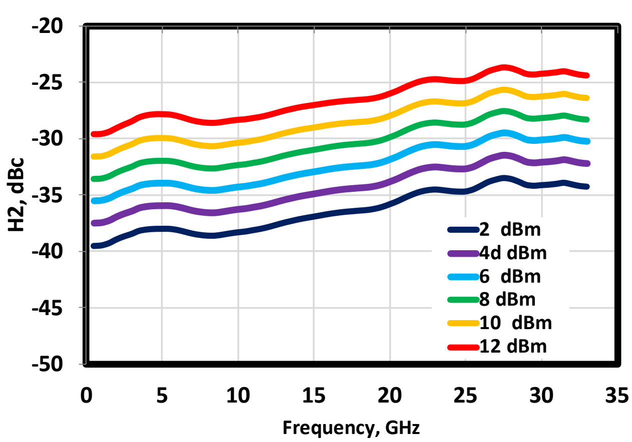


Figure 51 - 2-nd Harmonic vs. Power @ 7V/200mA

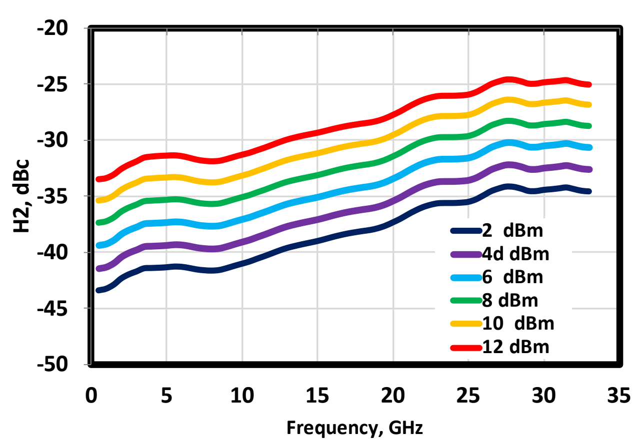
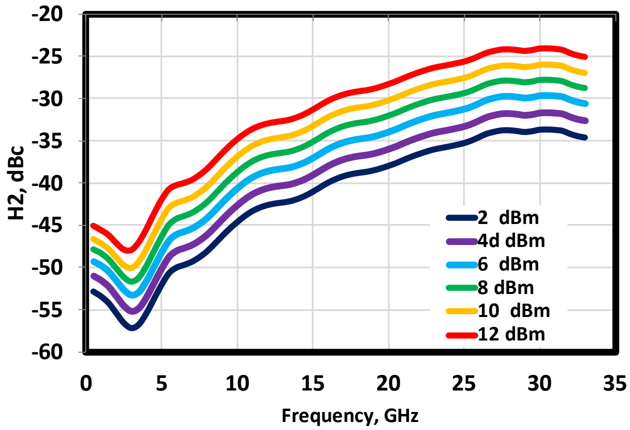


Figure 52 - 2-nd Harmonic vs. Power @ 8V/300mA



1.4. Die Specifications

The following illustration shows the chip outline of the MMA121AA device. Dimensions are in millimeters and are relative to the zero datum locations shown in the drawing. Nominal Die dimensions are 2.05x1.43x0.1 mm. The minimum bond pad size is 0.1 mm × 0.1 mm. Both the bond pad surface and the backside metal have 3 µm thick gold. The die thickness is 0.1 mm. The backside is the DC/RF ground. The airbridge keep-out polygon region is shown inside.

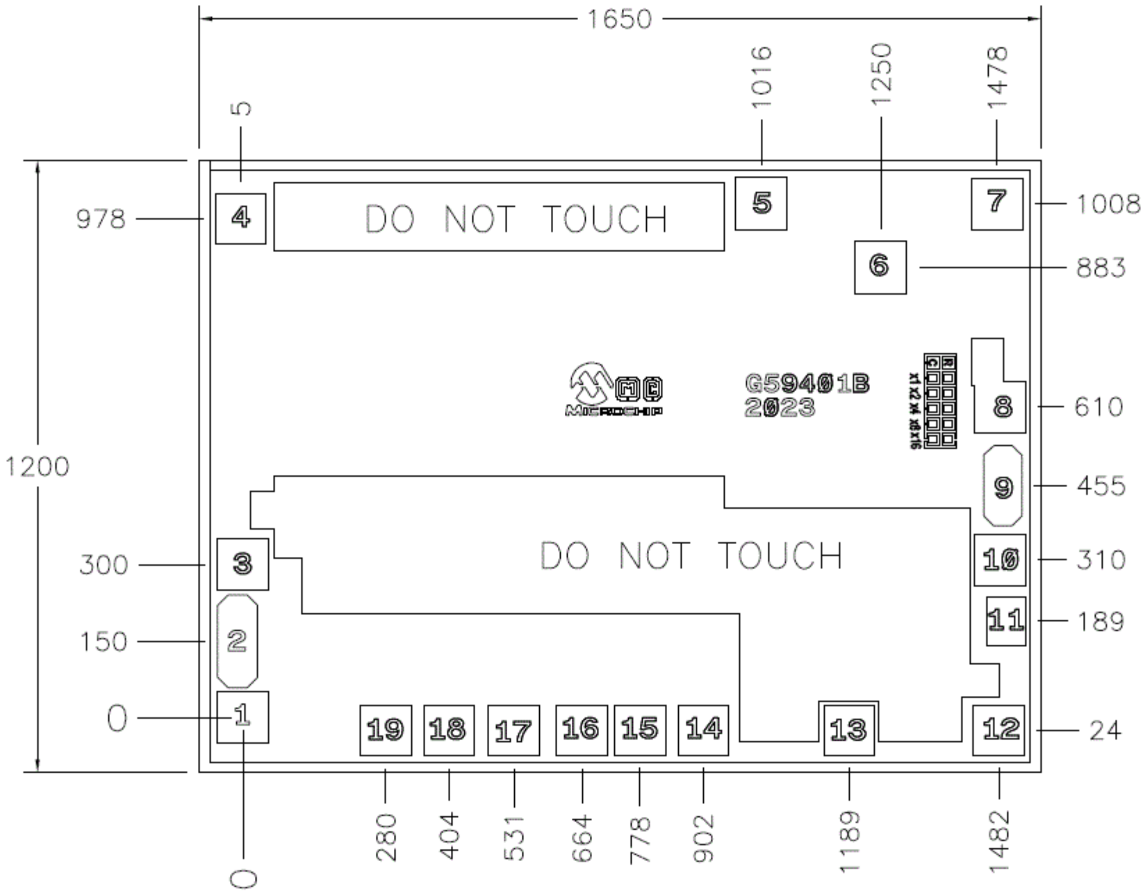


Figure 53 - Die Outline Drawing (um)

Table 3 - I/O Description

Pad Number	Pad Name	Pad Description (Effective Pad Size in um)
2	RF_{IN}	This pad RF/DC coupled to the FET Gates and matched to 50 Ohm (73x178)
9	RF_{OUT}	This pad is RF/DC coupled to the FET Drains and matched to 50 Ohm (70x152)
4, 5	V_{DDB} ,V_{DDA}	V_{DDA} ,V_{DDB} Low-Frequency Termination for Drain Ballast, DC Coupled to the FET Drains (96x96)
6	V_{DD}	V_{DD} Bias Pad (96x96)
11	V_{G2}	Access to Gate 2 Bias (70x90)
12, 14	V_{G1A}, V_{G1}	First Gate Low Frequency Terminations DC Coupled to the Gate 1 and used to set the Die Bias Current (96x96)
15,16, 17, 18, 19	V_{G1B},V_{G1C}, V_{G1D},V_{G1E}, V_{G1F}	Complimentary Low Frequency Terminations for the Gate 1, used to control low-frequency response slope (96x96)
1,3,7, 8, 10, 13	Ground	Ground connections used for die test purposes; DC/RF Ground is using Die Backside metal (96x96)

2. Application Circuits

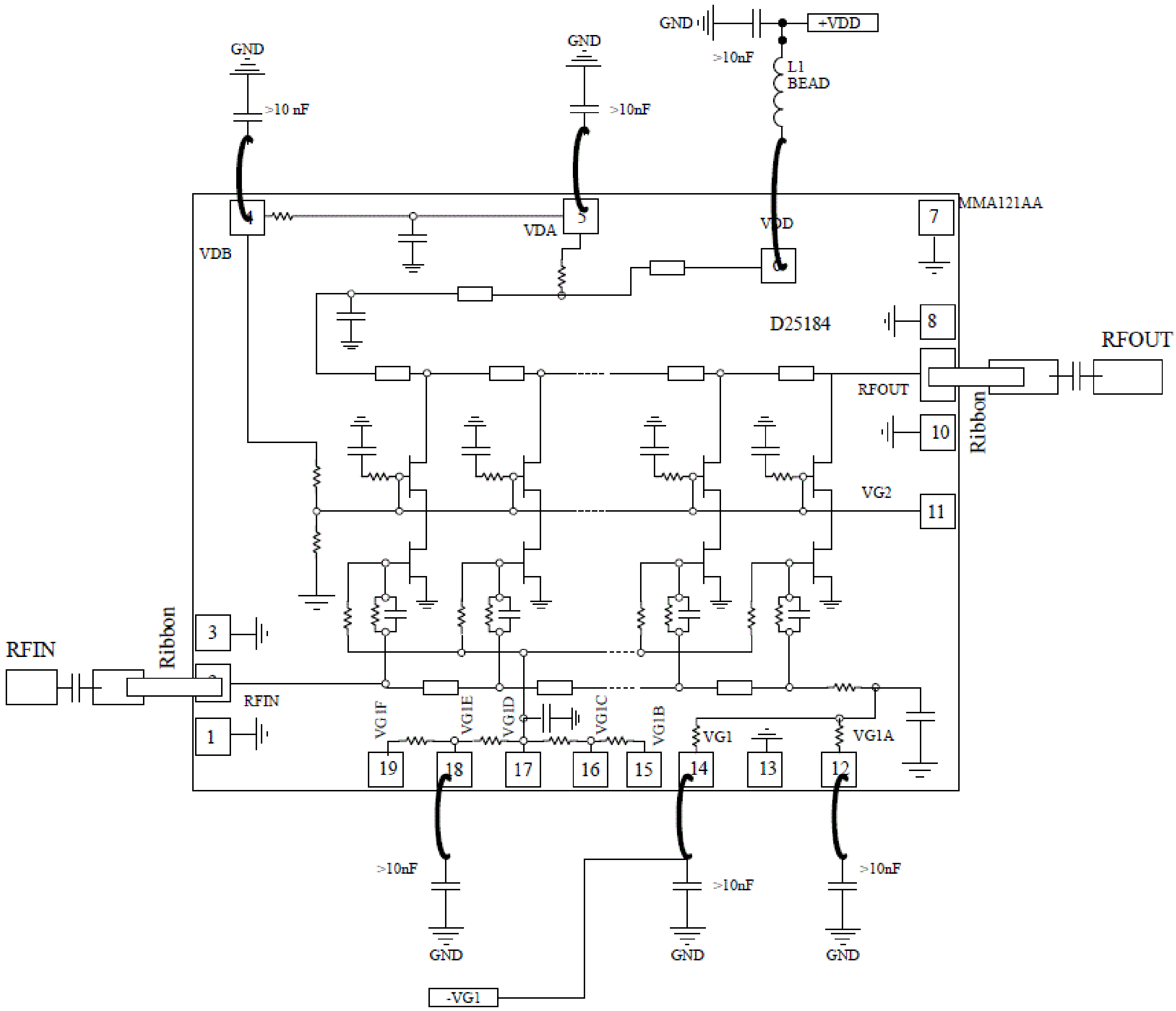


Figure 54 - Application Circuit: Schematic

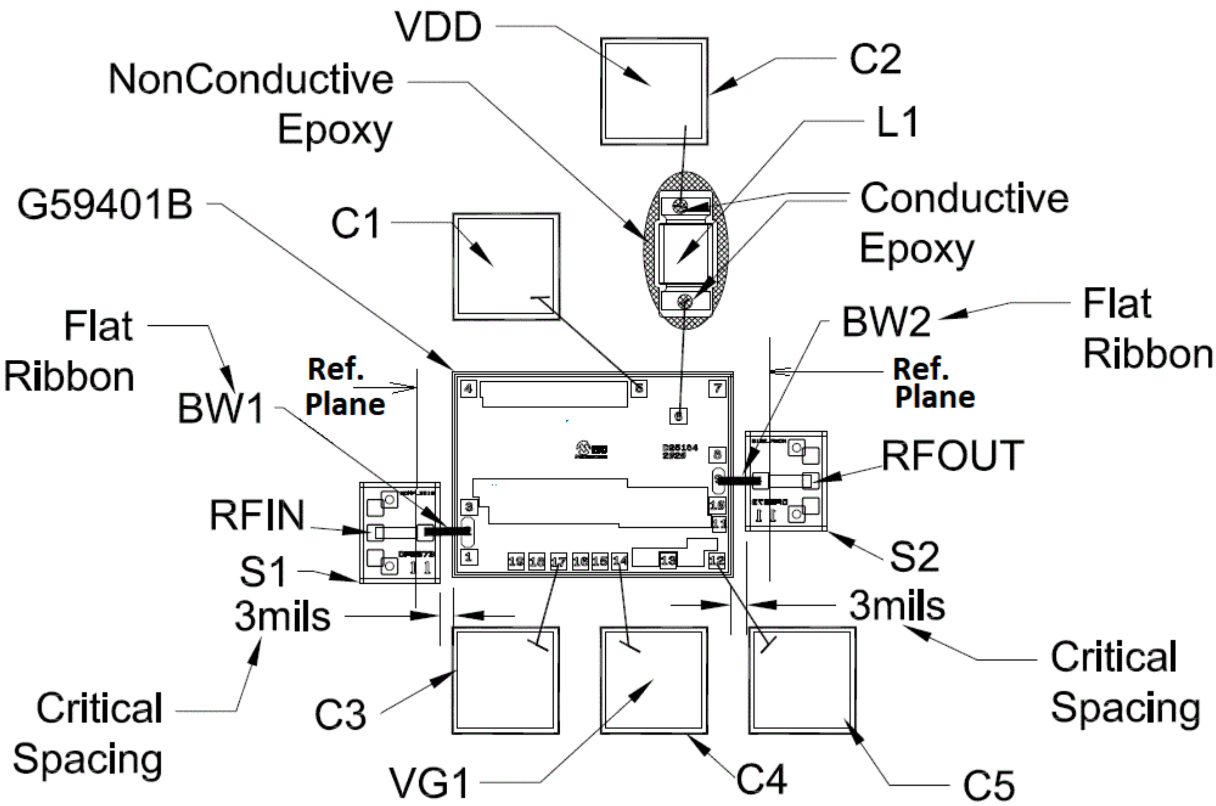


Figure 55 - Die Test Circuits: Assembly Drawing

Table 4 – List of Material for Test Circuit

Reference	Part Number	Description
G59401B	MMA121AA	MMA121AA Amplifier Die
C1, C2, C3, C4, C5	160U02A102MT4W	Johanson Dielectric, Cer.Cap 1nF
S1, S2	E57311	Probe Launchers
L1	0201 AF-330XRK	Coilcraft 0201 Ferrite Inductor
Epoxy	EpoTech H20E	Conductive Epoxy for die and cap mount

3. Handling Recommendations

Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

4. Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package
MMA121AA	Die

4.1. Packing Information

Standard Format
Gel Pack
50 Pieces per Pack

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